RADC SOI TEST FACILITY UPGRADE

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RCA Missile and Surface Radar Division

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This report describes the effort expended in upgrading the Wideband Pulse Compression Radar at the Floyd Test Annex to a 500 MHz bandwidth. The effort consisted of; transmitter redesign and overhaul, design and fabrication of a high speed system synchronizer, design and fabrication of a solid state sweep generator, and the installation and integration into the system of Government supplied equipment from other vendors. The Government furnished equipment included new; pulse compression filters, transversal equalizers,

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pulse compression dispersive delay line assembly, wideband RF front end including RF preamplifiers and several IF amplifiers. The major requirement and major work effort was; the achievement of very high system linearity, good stability and RFI avoidance.

RADC SOI Test Facility Upgrade

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J. E. Jackson

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This technical report has been reviewed and is approved.

Richard A. Ackley

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RADC Project Engineer

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SECTION 1
REPORT SUMMARY

During the period January 1973 to May 1974, RCA Corporation, in conjunction with Riverside Research Institute and the Rome Air Development Center, was engaged in a program to upgrade the RADC SOI Test Facility at the RADC Floyd Site near Rome, New York.

RCA's primary task was to integrate various critical systems components that were purchased by RADC and to supply a low-jitter master synchronizer. This necessitated the purchase by RCA of the components and cabinets necessary to complete this integration effort. In addition an RF computer-controlled checkout system for system calibration was designed and installed.

Several delivery problems were encountered with the RADC-supplied vendor components due to the rigorous specifications that were essential if low-level sidelobes ($>$ 30 db for this 500 MHz bandwidth radar that operates at S Band (3350 MHz)) were to be achieved. These problems were generally small but time-consuming to resolve.

Consequently most of the subsystem testing (but only limited system testing) was performed prior to contract completion.

One of the most critical components is the wide band sweeper (500 MHz BW at 2.46 GHz). The original sweeper used a voltage-tuned magnetron with a 1-watt output. These tubes are obsolete and no longer available from the vendor. RCA developed a solid-state sweeper to allow the program to proceed.

As a result of this program the synchronizing system was completely rebuilt; the low-level receiver processing was rebuilt; the antenna-located signal-frequency receiver system was rebuilt in an RFI-free cabinet; an additional room on the antenna was environmentally controlled; a wideband solid-state sweeper was built and installed in this room and the transmitter pulse width was widened to 40 usec in addition to obtaining the full 500 MHz capability of the transmitter.

This report deals with all these areas and is categorized as follows:

<u>System Improvements</u> (SECTION 2)

This section deals with the various components and changes that were planned and made and their impact on overall system performance.

<u>Site Technical Activity</u> (SECTION 3)

This section discusses the original work that was directly accomplished on site to support the purchased systems components and the wideband sweeper development.

Vendor-Supplied Components (SECTION 4)

The inclusion of this section is to provide a collated summary of the key features of the various key vendor-supplied components. The individual vendors each supplied their own instruction handbooks and the data in this section is intended to provide an overview of all these items which were supplied by five different companies.

Conclusions (SECTION 5)

This section presents a brief summary of the contract with conclusions drawn from the efforts performed.

During the program a total of 14 Program Memos were written and distributed. Most dealt with trip reports and recommendations based on those trips. However three of these reports are technically significant and, in the case of PGM 12, provided the results of an extensive set of transmitter measurements. The three are referenced throughout the text as existing documents; copies will be supplied by RCA to the interested reader upon inquiry to the authors.

SECTION 2
SYSTEM IMPROVEMENTS

2.1 General. In a wide band pulse compression radar such as the RADC SOI Test Facility, two of the most significant parameters in determining quality of the massive array of wide band components employed are amplitude ripple or flatness and phase ripple or linearity. As Klauder has shown by his paired-echo concept,[1] the level of time-sidelobes in a chirped radar system is a direct function of the amplitude and phase ripple. The relationship is shown in Figures 2.1 and 2.2.

Amplitude and phase ripple in radar systems are generally traced to the reflection of energy and the resultant voltage standing waves caused by the mismatching of contiguous components such as amplifiers, filters, mixers and the like. Figure 2.3 shows the time-sidelobe levels due to mismatch of two components having $VSWR_1$ and $VSWR_2$, respectively.

As an example, it can be seen that to achieve time-sidelobe levels of 40db, it is required that the two contiguous components in question each have a VSWR of 1.22, as seen from the intersection of the line marked "Line of equal VSWR pairs" with the curve labeled 40db Sidelobe Level.

In the case of unequal VSWR's, one can either predict the VSWR of the second component if the VSWR of the first and the sidelobe level are known by using the curves of Figure 2.2. Conversely, if the VSWR's of both components are known, the expected time-sidelobe level can be read from the curves. For example, if one component has a VSWR of 1.22 and the other contiguous component has a VSWR of 2.0, then a sidelobe level of 30db can be expected from this pair.

In order to measure and evaluate components and even subsystems several test loops have been devised for the test facility involving both the wideband and narrowband swept signal as well as a narrow pulse (2 nanoseconds) generated in the time domain.

2.2 Test Loops. Basically, three internal test loops have been incorporated into the radar system, to allow system calibration and adjustment as well as monitoring performance and locating defective components. These three loops operate at 1) 3350 MHz F_o, with a 500 MHz chirped 40 usecond pulse, 2) 950 MHz, with a 2.5 MHz chirped pulse and 3) 45 MHz with a 2.5 MHz chirped pulse. Each of these loops utilizes switches driven by TTL logic and have been interfaced with the PDP-1 computer to provide computer-controlled static and dynamic internal test data.

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1 "THEORY AND DESIGN OF CHIRP RADARS" - Klauder, Price, Darlington, Albersheim, Bell Telephone System, Monograph 3660.

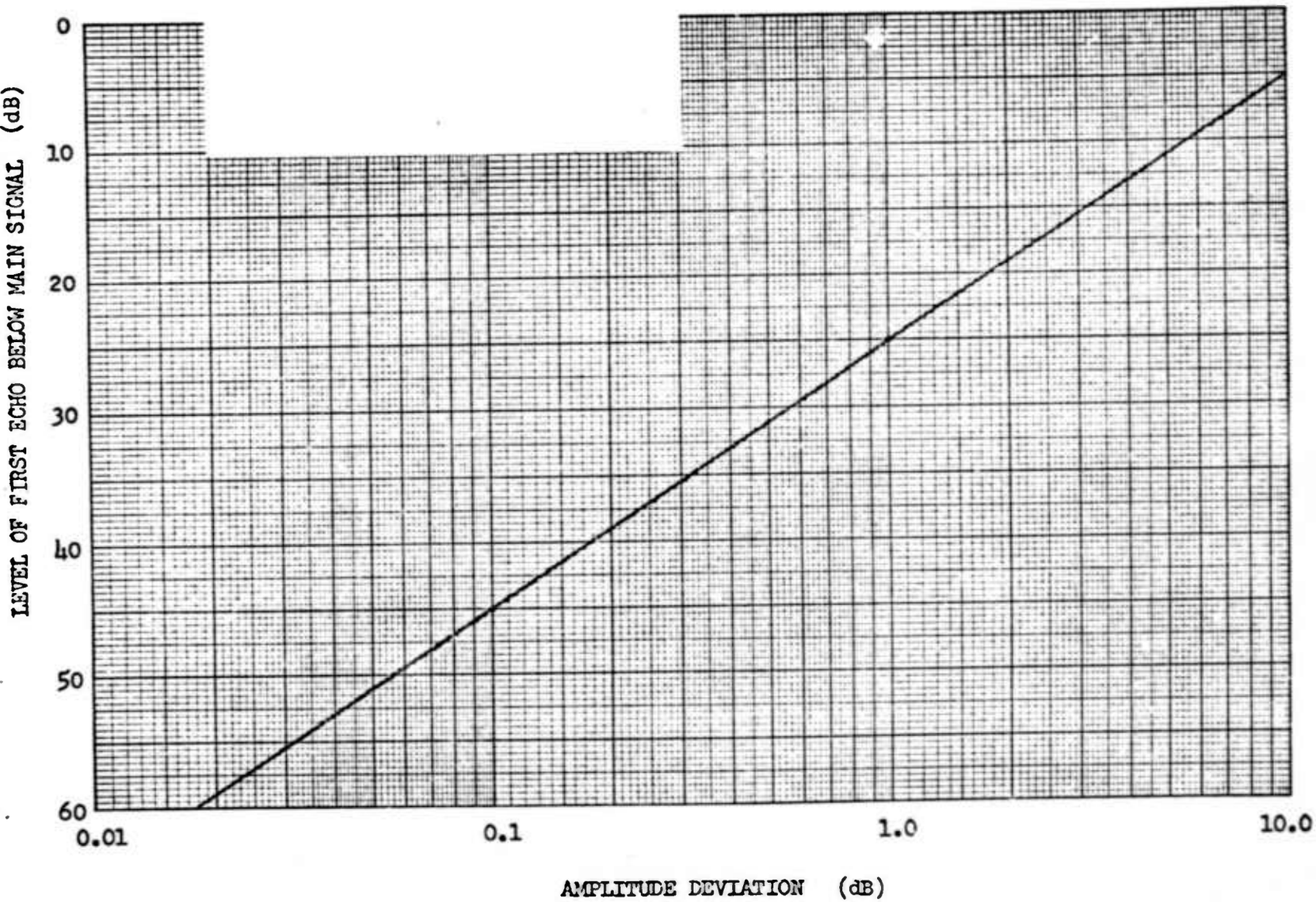

Figure 2.1 Amplitude Echoes

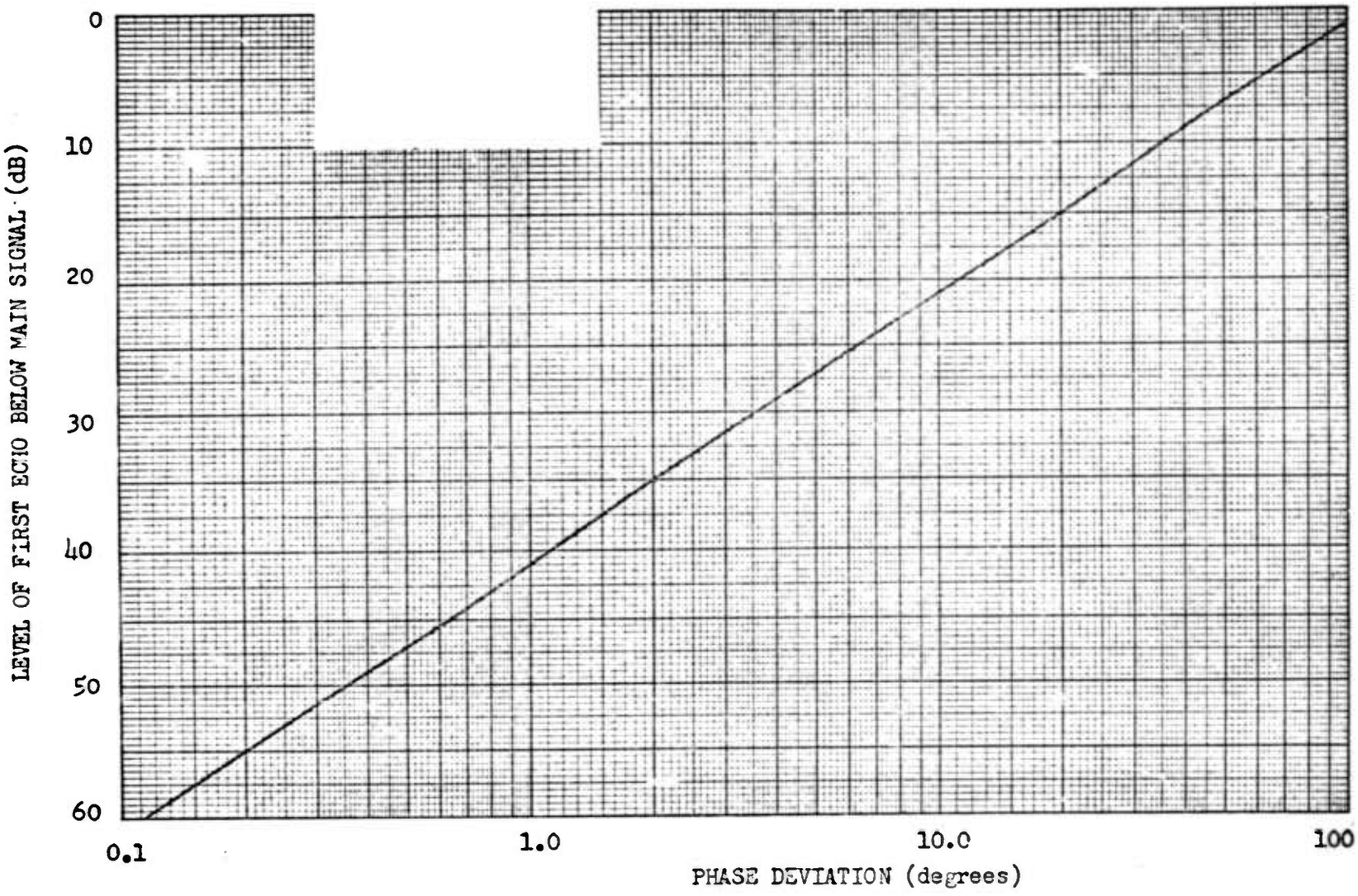

Figure 2.2 Phase Echoes

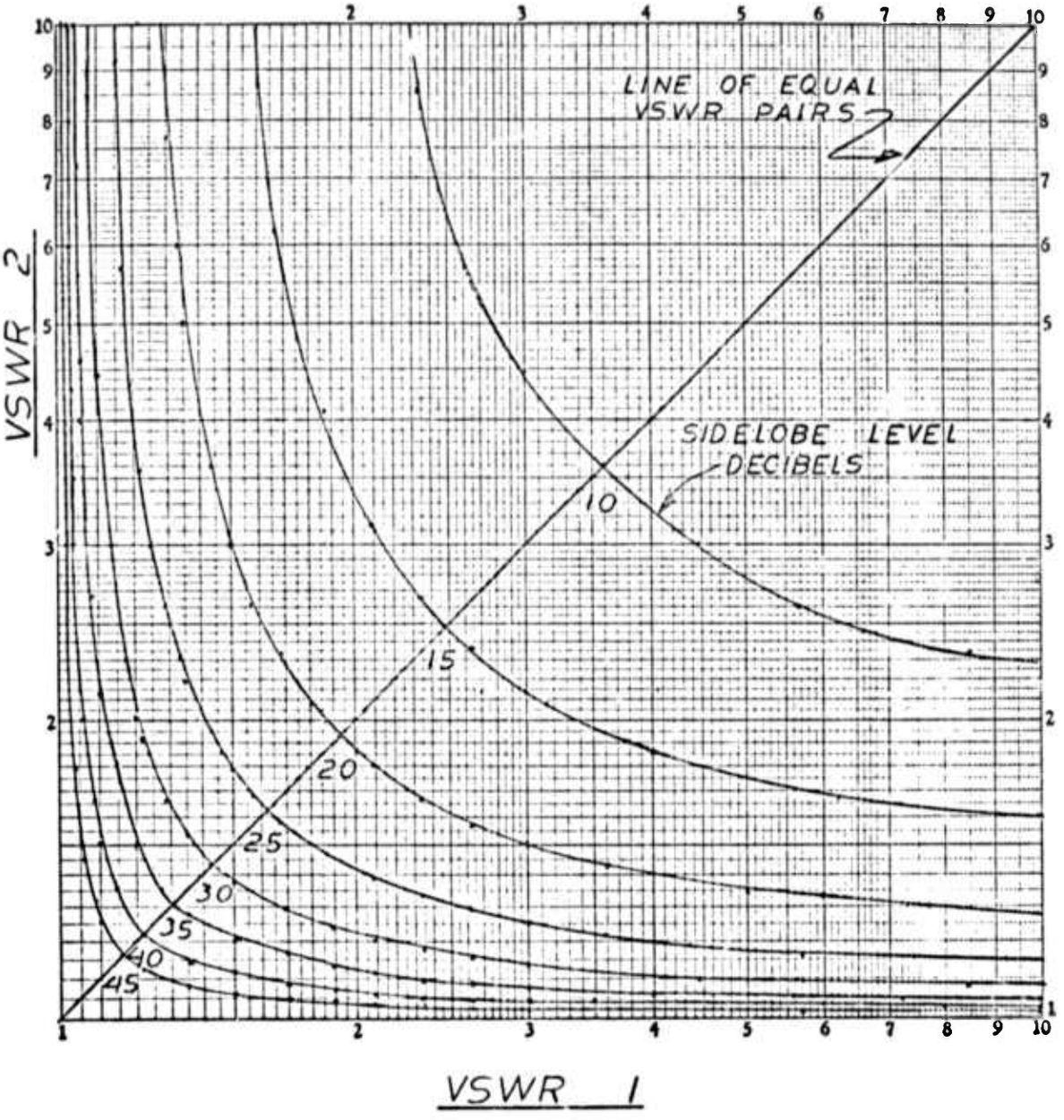

Figure 2.3 Time-sidelobe Levels for Different VSWRs

The RF or 3.35 GHz test loop also contains a solid-state noise source to allow the measurement of system noise figure as well as minimum discernible signal for a sensitivity measurement. Figure 2.4 is a block diagram of the 3.35 GHz swept signal and noise test loop.

Each of the switches shown in Figure 2.4 can be actuated either by the system computer or by manual switch. They are connected normally in the fail-safe mode; that is, with loss of power, the switches will revert to the signal thru-path rather than a test path.

Thus, noise figure is measured by energizing S_2, S_4, S_5, S_6 and S_7, with S_3 in the "off" position. RMS noise value is measured at the video end of the receiver. S_3 is then energized, firing the noise source, and another reading taken of the noise power at the same point in the receiver. The output attenuator is then adjusted until the noise power reading with the source "ON", is the same as that with source "OFF". The change in attenuation is the "Y" factor, and Noise Figure can be computed from the following relation:

$$F(db) = 10 \log \frac{ENR-1}{Y-1}$$. Where ENR is the effective excess noise ratio of the noise source as seen at the input to the preamplifier being measured.

To measure sensitivity, the test signal at 3350 MHz is injected into the pre-amp by energizing S_1 and adjusting the attenuator in series with the test signal until the signal reaches some pre-arranged value.

T-R tube recovery time can also be monitored or measured in this manner by emitting a transmit pulse from the antenna, thus firing the T-R tube. Secondly, a test signal is injected into the receiver and stepped closer in range until its level as measured at the receiver output is attenuated by some predetermined level, usually 3 db. The time between the end of transmit pulse and the beginning of the test pulse is then the recovery time of the front end, principally the T-R tube.

For the first IF and second IF test targets, a frequency synthesizer is used to effect a slope reversal of the dispersed pulse and provide a moving target that can be slewed or stepped throughout the entire 2.5 MHz window as determined by the computer program. In addition, the computer commands the programmable attenuators normally used for AGC in the vertical and horizontal IF channels to simulate a target varying in amplitude.

Since the synthesizer is controllable in steps as small as 0.01 cycle, the test target can be used for phase measurements and calibrations as well as amplitude measurements and calibrations.

The 45-megahertz test-target generator block diagram is shown in Figure 2.5.

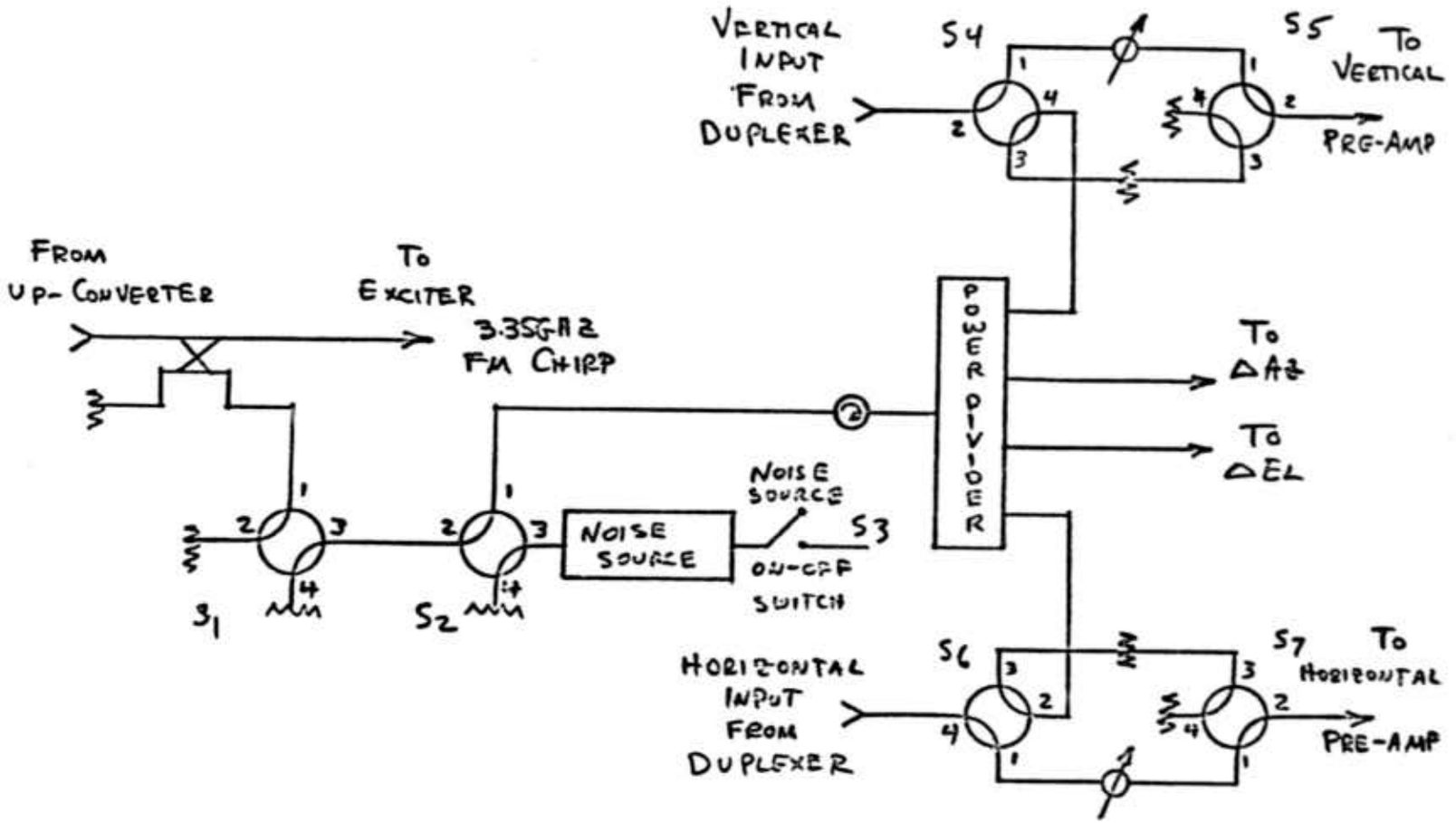

Figure 2.4 Noise and Wideband Signal Test Loop

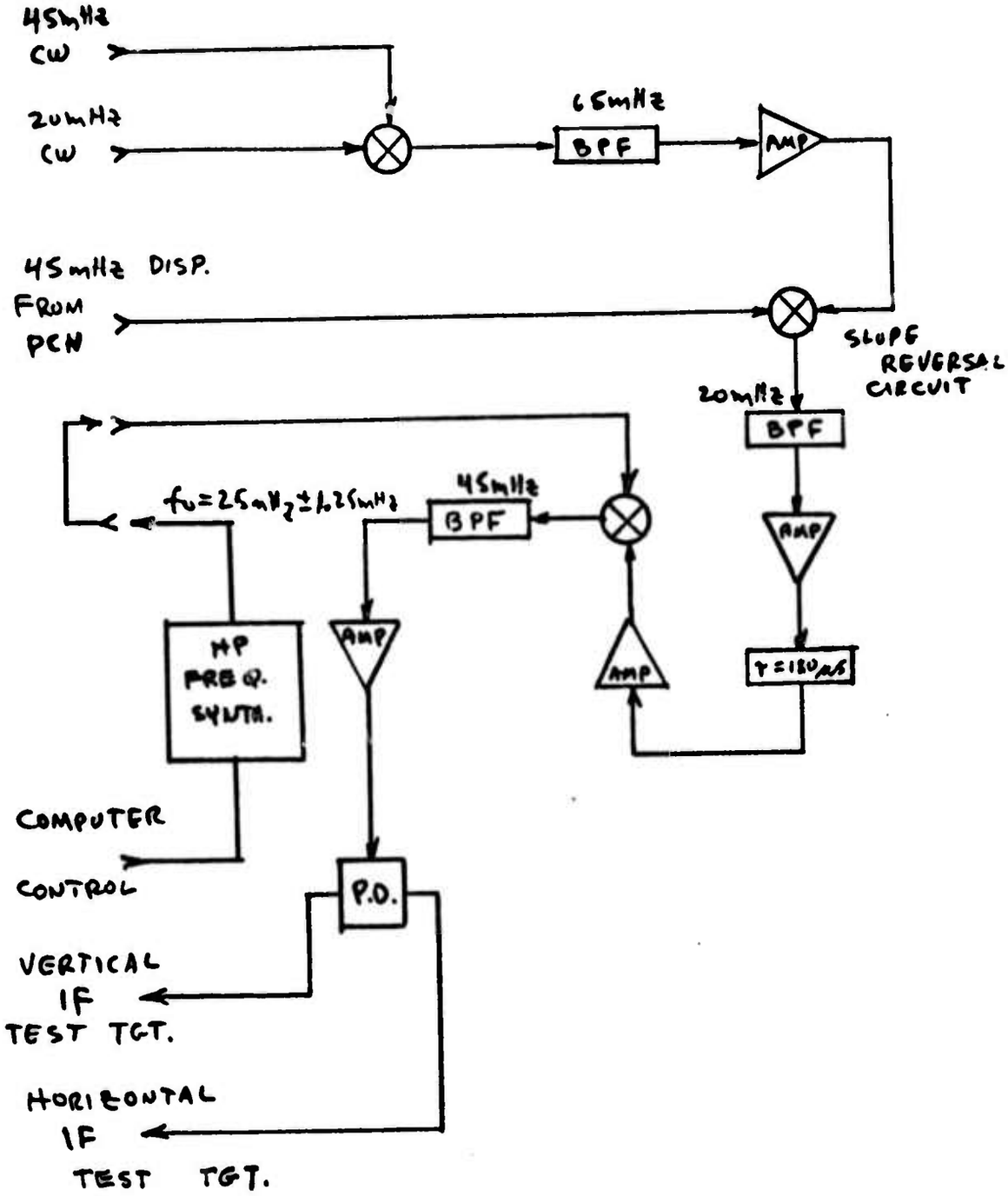

Figure 2.5 Block Diagram, 45-MHz IF Test Target Simulator

The first IF, centered at 950 MHz, receives its test target signal from the up converter, where the 45 MHz computer-controlled signal is mixed with 995 MHz. A sample of this signal is taken by means of a 10 db directional coupler and fed to a power divider for insertion to the vertical and horizontal IF channels as shown in Figure 2.6.

2.3 Solid State Sweeper. Originally, the test facility had utilized a voltage-tuned magnetron as the source for the 500 MHz-bandwidth FM chirp pulse. This approach was found to be inadequate for several reasons: 1) the tube and associated circuitry were optimized for 250 MHz Bandwidth operation; 2) magnetrons themselves are inherently unstable; 3) to increase the bandwidth to the necessary 500 MHz, the voltage ramps would have to be modified to produce sawtooths ranging as high as 500 volts peak-to-peak, increasing the probability of EMI; 4) space required for the VTM configuration was quite large creating a physical space problem; 5) the tube used is obsolete and reengineering would be required to use an alternate type.

In view of the above, a solid-state voltage-controlled sweeper was procured by RADC, but due to numerous difficulties by the supplier, it was decided to design an interim, open-loop sweeper in order to complete the installation and to conduct tests using external as well as internal targets.

Because of the lack of time and money, an approach was taken that would most expeditiously tie the radar together as a system, albeit with reduced performance. Hence, a solid-state voltage-controlled oscillator was ordered from Solid State Technology and incorporated into a three-bandwidth sweeper centered at 2.4 GHz.

Data taken on the VCO indicated less than 1% (0.7%) deviation from linearity of the voltage/frequency characteristics as shown in Figure 2.7, plotted from the data taken in Table 2.1. Although this data was taken passively, in the CW mode, the accuracy of the linearity was corroborated by a dynamic Linearity Measuring Technique described in FOM-17, Reference 3.

The VCO characteristics are: 1) Linearity (frequency versus voltage) - 0.6%; 2) Amplitude Ripple (flatness) +0.3 db; 3) Power Output: +23dbm; 4) Voltage Sensitivity: 125 KHz/millivolt.

This VCO unit was incorporated in the wide-band sweeper described in subsection 3.6.

2.4 Range Tracker Look-Ahead. Because of the limitations of the existing range tracker, a look-ahead scheme was developed to allow lock-on of the target in the wideband mode. Its operation is as follows: after acquisition of the target in the CW mode, the system reverts to an interlaced mode, where the CW signal is radiated for angle-tracking purposes while every other radiated pulse is one of the three selected bandwidths, 5 MHz, 50MHz or 500MHz. Since the range tracker requires one to two seconds to settle out, it is highly doubtful based on past experience that the lag errors would be sufficiently reduced when the bandwidth was increased to provide a narrower range window.

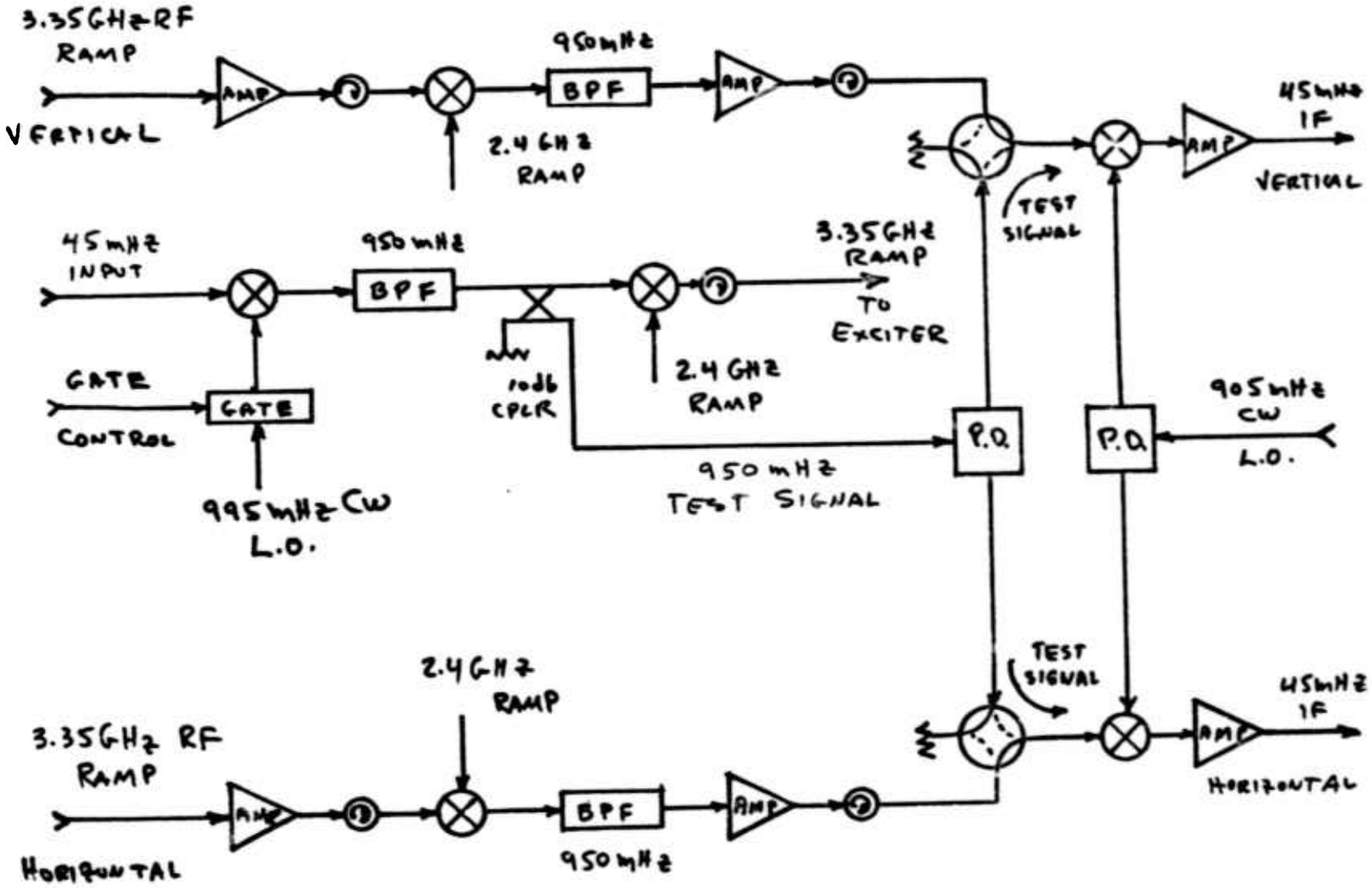

Figure 2.6 950-MHz IF Test Signal Sampling Circuit

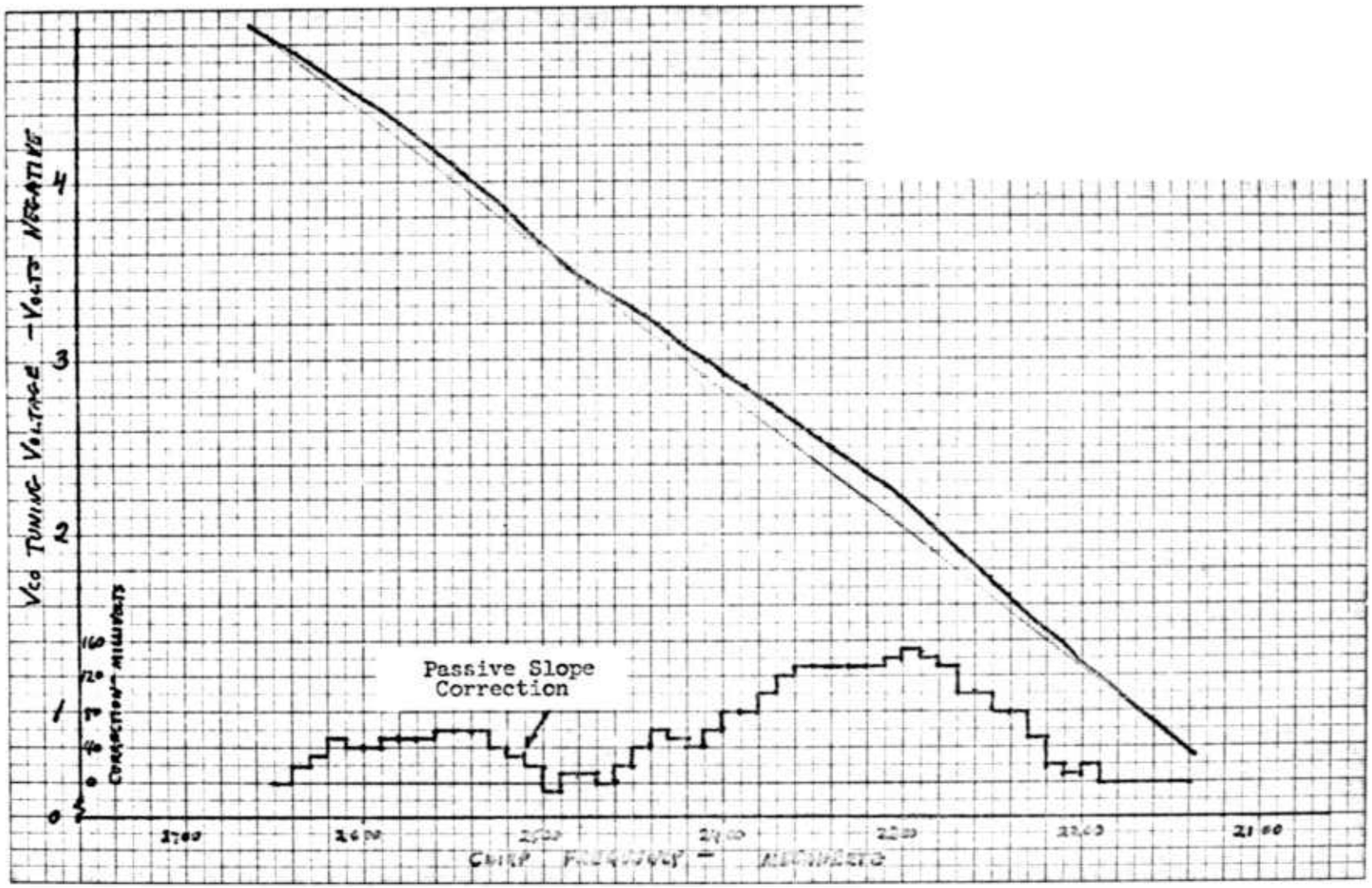

Figure 2.7 Solid-State VCO Performance Data

TABLE 2-1 SOLID-STATE VCO PERFORMANCE DATA

SSV - 0266 LI , Serial Number I

VOLTS	FREQUENCY	VOLTS	FREQUENCY	VOLTS	FREQUENCY	VOLTS	FREQUENCY
.150	2059.28	1.45	2221.16	2.75	2373.32	4.05	2543.73
.20	2065.66	1.50	2226.42	2.80	2380.69	4.10	2549.64
.25	2071.40	1.55	2231.67	2.85	2387.65	4.15	2556.23
.30	2077.46	1.60	2236.63	2.90	2394.93	4.20	2562.34
.35	2083.40	1.65	2241.71	2.95	2403.33	4.25	2568.54
.40	2090.10	1.70	2246.34	3.00	2411.01	4.30	2574.75
.45	2096.55	1.75	2251.84	3.05	2419.11	4.35	2581.29
.50	2104.20	1.80	2258.30	3.10	2425.15	4.40	2587.71
.55	2111.32	1.85	2263.40	3.15	2429.99	4.45	2594.33
.60	2118.51	1.90	2268.06	3.20	2435.63	4.50	2601.16
.65	2125.40	1.95	2273.32	3.25	2442.42	4.55	2609.18
.70	2131.63	2.00	2278.40	3.30	2450.41	4.60	2616.08
.75	2137.55	2.05	2283.82	3.35	2460.60	4.65	2623.47
.80	2143.05	2.10	2289.30	3.40	2469.59	4.70	2630.76
.85	2148.01	2.15	2294.96	3.45	2477.51	4.75	2638.25
.90	2154.19	2.20	2301.76	3.50	2483.83	4.80	2645.97
.95	2160.25	2.25	2307.96	3.55	2489.53	4.85	2653.48
1.00	2166.95	2.30	2314.14	3.60	2494.84	4.90	2662.16
1.05	2173.20	2.35	2320.57	3.65	2500.13	4.95	2669.80
1.10	2179.52	2.40	2326.78	3.70	2508.48	5.00	2677.72
1.15	2185.78	2.45	2333.04	3.75	2510.71	5.05	2686.29
1.20	2191.83	2.50	2339.26	3.80	2515.92	5.10	2693.81
1.25	2197.73	2.55	2345.59	3.85	2521.27	5.15	2703.12
1.30	2203.66	2.60	2352.00	3.90	2526.77	5.20	2711.45
1.35	2209.48	2.65	2359.55	3.95	2532.57	5.25	2721.82
1.40	2215.15	2.70	2366.16	4.00	2538.14	5.30	2729.54

The look-ahead feature allows the radar to track in one mode, say 5 MHz, while displaying the video of the next wider bandwidth (50 MHz). Any range error observed in the wider bandwidth is removed by means of a "joy-stick" with memory, so that the "look-ahead" target is centered in the range window. When the range error is suffieiently reduced, the 50 MHz bandwidth is selected for range tracking and the 500 MHz is displayed in look-ahead fashion. The process is repeated until the target is locked in range in the widest bandwidth (narrowest range window).

2.5 Programmable AGC. The receiver AGC was modified to allow 95-db dynamie range in 4-db steps insertable automatieally by the computer. This is an improvement in the dynamie range of 35 db over the former scheme. Added are a switehable 32-db attenuator ahead of the RF pre-amp to prevent saturation of the front-end on strong signals, and a T^2l compatible programmable attenuator manufactured by Daico Industries in the 45-MHz IF. Both of the attenuators have switching times of about 10 usec, so they can be switehed at a PRF rate if neeessary, as may be the case in rapidly tumbling spaee objects.

These attenuators are switched by the computer during measurements made in the internal tests using the internal test target simulator as well as in real time operation.

2.6 Waveguide Dispersion Correction. According to Elliott[1], phase veloeity in a waveguide is a nonlinear function of frequeney and thus causes dispersion of the spectral components in the pulse waveform. In one assumes that in most practieal eases, the phase constant is a quadratie function of then B(w), the phase constant can be expressed by:

$$B(\omega) = \frac{2\pi}{\lambda_g} = \frac{\sqrt{\omega^2 - \omega_c^2}}{v} \qquad (1)$$

where, λ_g is the guide wavelength at the angular frequency w and $v = \frac{1}{\sqrt{\mu e}}$, with μ and e the permeability and permittivity, respeetively, of the mediums, filling the guide. ω_c is the eut off angular frequeney of the particular mode being considered.

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1. "Pulse Waveform Degradation Due to Dispersion in Waveguide", IRE Transactions on Microwave Theory and Techniques. Oetober 1957 - pp. 254-257.

Eq (1) can be expanded in a Taylor's series about the angular frequency ω_o, giving

$$\beta(\omega) = \beta_o + \frac{\omega_o}{v^2 \beta_o}\left[\omega - \omega_o\right] - \frac{1}{2}\frac{\omega_c^2}{v^4 \beta_o^2}\left[\omega - \omega_o\right]^2 + \frac{1}{2}\frac{\omega_o \omega_c}{v^6 \beta_o^5}\left[\omega - \omega_o\right]^3 - \cdots \quad (2)$$

It is apparent from (1) and (2) that $B(\omega)$ is not a linear function of ω. Thus, the Fourier components of a pulse travelling down the waveguide are dispersed, and the exit waveform is degraded. The amount of degradation depends on the Fourier composition of the waveform, the length "L" of the run of waveguide, and the rapidity of convergence of the series (2).

A convenient method of compensation for the dispersive effects of the waveguide run is to run the wide band L.O. signal through an equivalent length of waveguide, thus equalizing the instantaneous time delay throughout the pulse.

Equation (1) can be rewritten to

$$\beta(\omega) = \frac{L}{c}\sqrt{\omega^2 - \omega_c^2} = \phi \quad (3)$$

where L = length of guide, c = speed of light.

The equivalent instantaneous time delay is:

$$\tau = -\frac{d\phi}{d\omega} = -\frac{L}{c}\left(1 - \frac{\omega_c^2}{\omega^2}\right)^{-\frac{1}{2}} \quad (4)$$

Let $a = \frac{\omega_c}{\omega}$, then:

$$\tau = -\frac{L}{c}\left(1 - a^2\right)^{-\frac{1}{2}} \quad (5)$$

The rate of change of delay with the frequency variable is:

$$\frac{d\tau}{da} = -\frac{L}{c}\left(1-a^2\right)^{-\frac{3}{2}} \qquad (6)$$

Since $a = \frac{\omega_c}{\omega}$, $\frac{da}{d\omega} = -\frac{\omega_c^2}{\omega}$, then

$$\frac{d\tau}{d\omega} = \frac{L}{c}\,\frac{a^2}{\omega}\left(1-a^2\right)^{-\frac{3}{2}} \qquad (7)$$

A length of WR340, having an ω_c of 1.737 GHz will be calculated to provide the correction due to 30 feet of WR284 in the transmit path. WR284 has an ω_c of 2.08 GHz.

$$\frac{L_2}{c}\cdot\frac{a_2^2}{\omega_2}\left(1-a_2^2\right)^{-\frac{3}{2}} = \frac{L_1}{c}\cdot\frac{a_1^2}{\omega_1}\left(1-a_1^2\right)^{-\frac{3}{2}} \qquad (8)$$

$$L_2 = \frac{a_1^2}{a_2^2}\cdot\frac{\omega_2}{\omega_1}\left[\frac{1-a_1^2}{1-a_2^2}\right]^{-\frac{3}{4}} \qquad (9)$$

$$L_2 = 0.36\,L_1 = 0.36 \times 30\,ft = 10.8\,ft \qquad (10)$$

Thus 10.8 feet of WR340 was inserted in the L.O. line to effect the compensation.

A plot of the change in time delay due to both lengths of guide as well as the equalizing effect of the corrective guide shows that a 4-nanosecond dispersion is reduced to approximately 320 picoseconds (Reference 2). In corroboration, a 0.2-nanosecond pulse was fed through the corrective guide and its dispersed rate displayed on a sampling scope. The change in frequency with time shows the dispersive properties of the guide.

Figure 2.8 shows the parameters of the waveguide assembly as well as an outline sketch of the mechanical configuration.

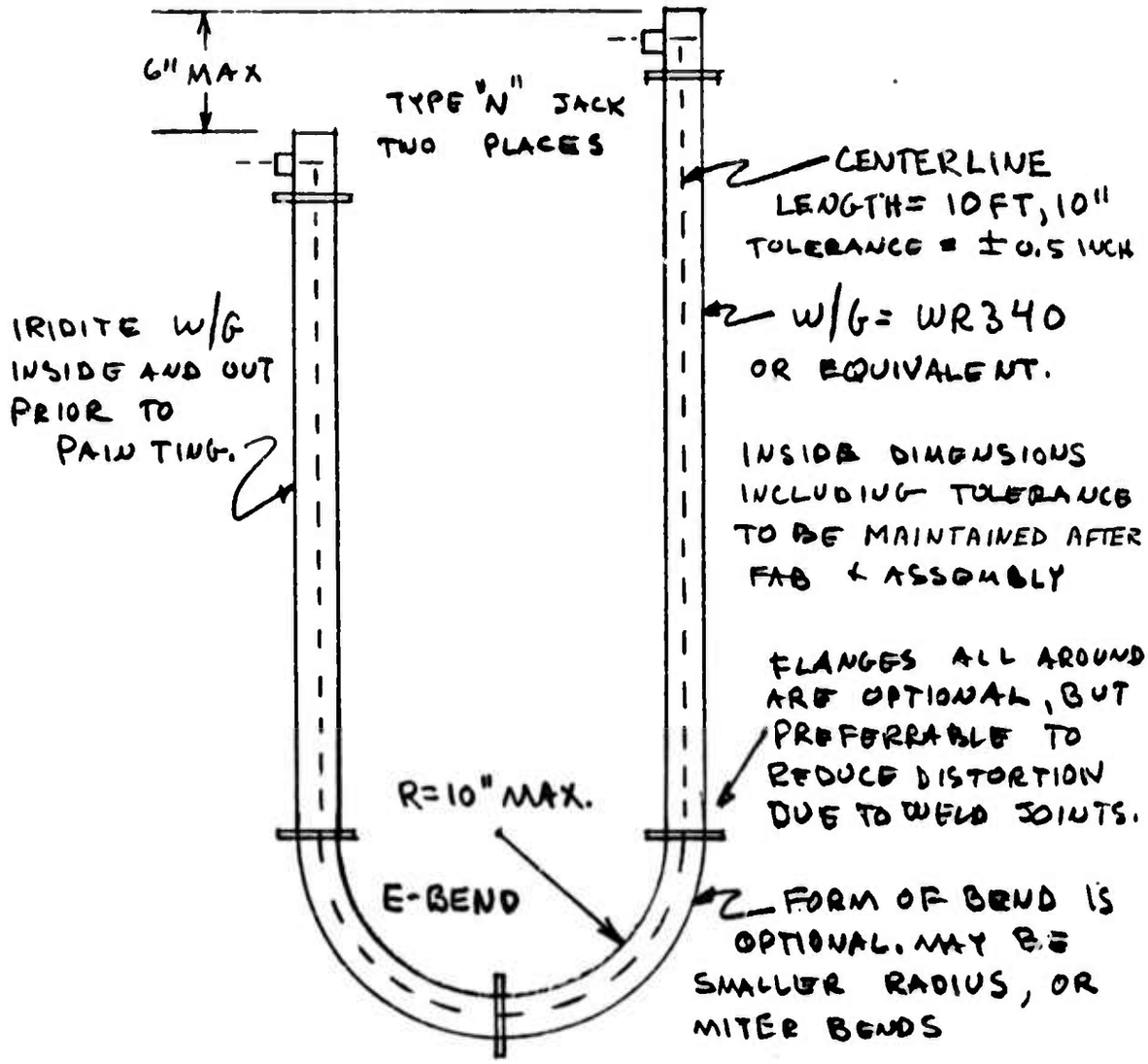


Figure 2.8 Specification CFC 618731, Waveguide Assembly, to be Used in a Dispersion Network in an S-band Radar.

SPECIFICATION CFC 618731
WAVEGUIDE ASSEMBLY

1. This Specification applies to a Waveguide Assembly to be used in a dispersion correction network in an S-Band radar.

2. Operating Frequency - 2.4 GHz nominal.

3. Bandwidth - 2.15 to 2.65 GHz.

4. Waveguide: WR 340 (Aluminum).

5. Connectors: Type N, Jack.

6. Flanges: Optional.

7. VSWR: 1.2 or less over band.

8. Paint: White all over except connectors.

9. Configuration: See Figure 2.8

When internal test targets are used, (no waveguide employed), the dispersion correction is bypassed and an equivalent length of 1/2" alumi-spline cable is substituted as shown in Subsection 3.2.1.

2.7 Phase-Locked Oscillators. During the test and measurement phase of the upgrading of the RADC SOI Test Radar, it was determined that the three high-order frequency multipliers used in the system be replaced by phase-locked oscillators. These are the 880 MHz, 995 MHz and 2.4 GHz multipliers which have multiplier constants derived from 5 MHz, of 176X, 199X and 480X, respectively.

The reason for their replacement was two-fold: 1) the inherent instability and level-sensitivity of these devices, and 2) the signal-to-noise ratio of the reference source is degraded by a factor of 20 log N, where N is the multiplication factor.

Thus, the degradation is 44.9 db, 45.9 db and 53.6 db respectively for the three multipliers. Since the 5-MHz source noise was down about 110 db, the degradation resulted in marginal performance if 40 db time sidelobes are to be attained.

The principal benefits from multiplier replacement are: 1) the "FM Noise" or deviation of the carrier is at least phase related to the source, and 2) the effects of the multiplied noise are separated from the desired carrier by the reference frequency or 5 MHz. In addition, with a cavity-type oscillator, circuit Q's of 1000 or greater can be achieved reducing the effective noise bandwidth and hence the total noise power in the output signal. Signal-to-phase noise ratios of greater than 85 db were attained with the phase-locked oscillators provided.

SECTION 3
SITE TECHNICAL ACTIVITY

Introduction. This section of the report is structured to describe the site activity which performed the detailed mechanical design and construction of the cabinets to accommodate the new major assemblies and their supporting equipment in addition to a development program for the wide band sweeper and an extensive set of measurements designed to optimize transmitter performance and convert it to 40 usec operation.

3.1 System, Hardware Configuration.

3.1.1 Processing Systems Block Diagrams. Figures 3.1 and 3.2 show the high and low frequency signal processing system. Figure 3.1 is the Wideband Front End (located in Unit 77 on the Antenna).

The 3350 MHz signal returns in vertical and horizontal (V&H) are supplied to this unit from the duplexer assemblies. The wide band ramp from Unit 74 is inserted at the correct time by the range tracker and synchronizer and beats down the target returns to the first IF of 950 MHz.

Test targets at 3350 MHz and 950 MHz can also be inserted by using switches SW1 and SW3 and A1, A5, respectively. SW2 and SW4 allow a 32db attenuator to be inserted for large targets. The 950 MHz first-IF signals are mixed with a nominal 905 MHz oscillator which is frequency shifted to remove the doppler shift on the returns.

This results in a 2.5 MHz Bandwidth IF at 45 MHz that is cabled from the pedestal to the low level signal processing system located at ground level.

This block diagram is shown in Figure 3.2. The pulse compression network is used both for transmission and reception. During transmit the unit is impulsed and uses the site 5 MHz reference to generate a 45 MHz pulse with a 2.5 MHz bandwidth using conventional gating to produce a Sin x/x function and a dispersive delay line to produce the swept pulse. This output is gated and used to drive the transmitter exciter.

To provide both V&H signals and economize in delay lines, these functions are time multiplexed by the use of fixed delay lines (80 and 130 usecs) in each receiver line. This causes the horizontal to be processed into the input port J3 50 usec later than the vertical receiver signal.

Following compression within the PC network the target data is outputted from J4; meanwhile a swept transmit-type waveform has been obtained from J8, gated, delayed and mixed to provide a deramping signal. This is mixed with the compressed pulse in mixer 23A4A6 and the time-multiplexed 20 MHz compressed target data supplied to 23A5 for subsequent processing through the transversal equalizer and recording in the DHE equipment.

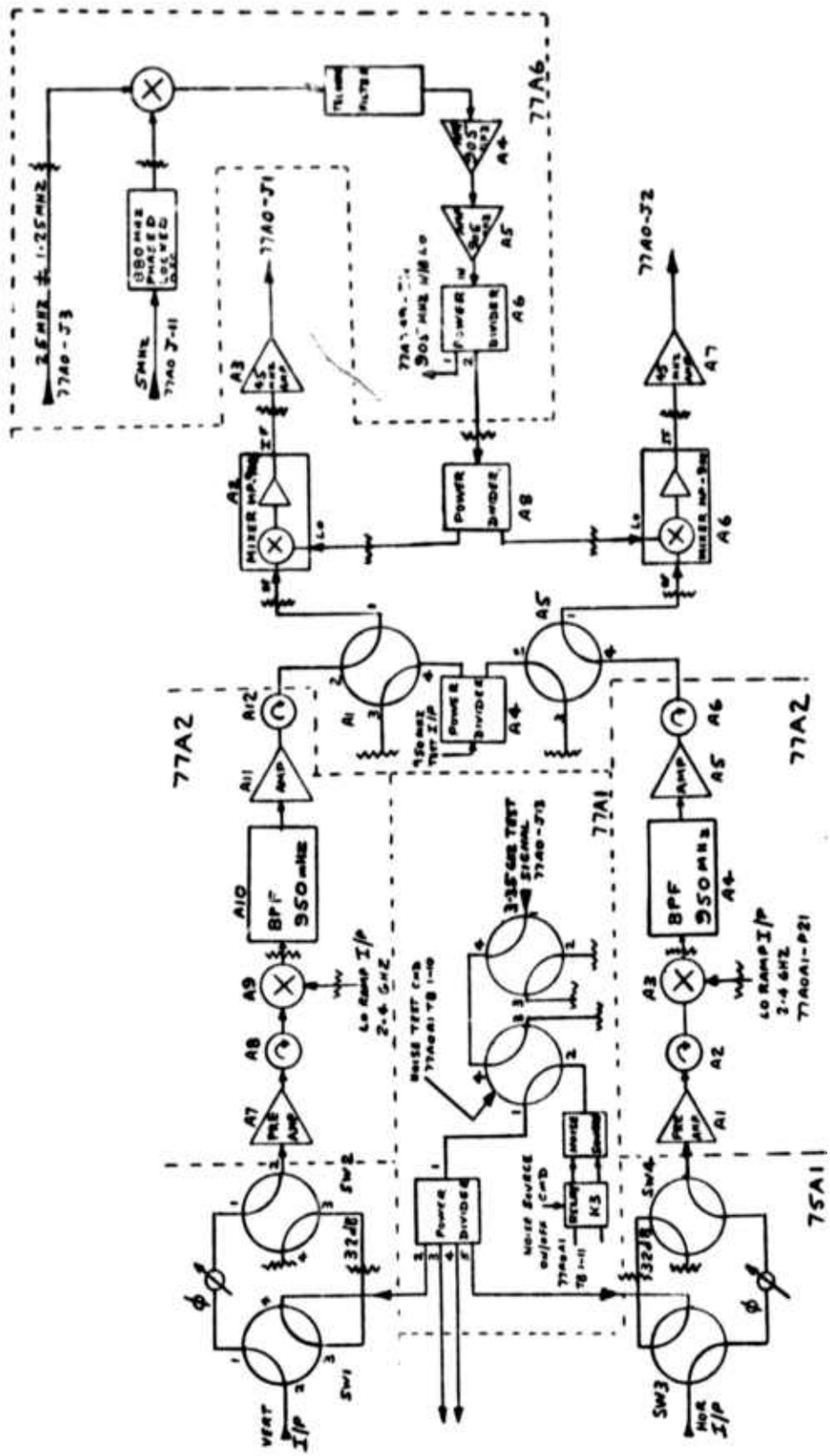


Figure 3.1 Wideband Front End, Unit 77

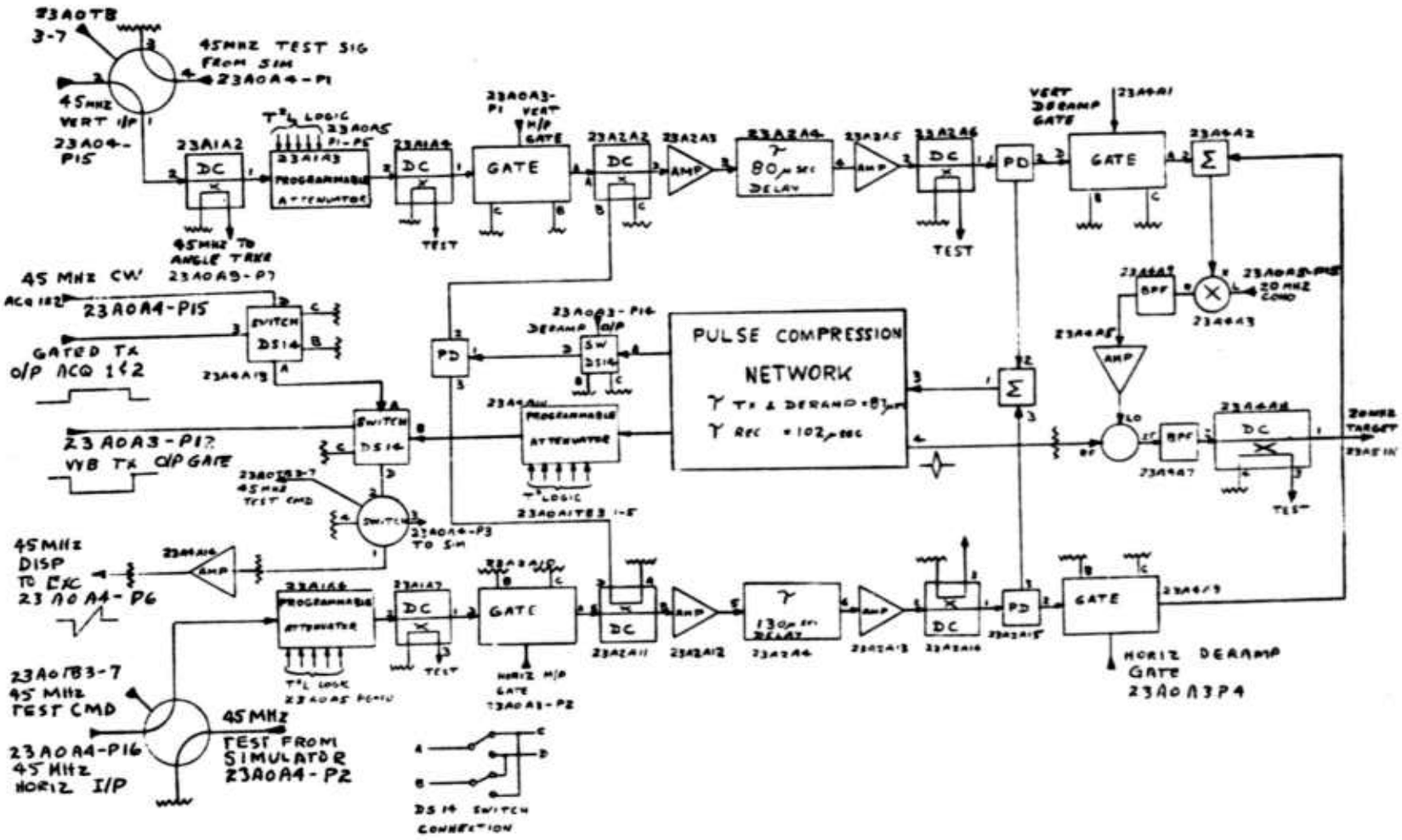


Figure 3.2 Signal Processing Block Diagram

3.1.2 System Modes. The system has several modes of operation. These can be segregated into two main areas, aequsition and test.

3.1.2.1 Aequisition Modes. Figure 3.3 shows the various system modes. ACQ 1 is the basie acquisition with system unloeked and the antenna pointed by the computer. ACQ 2 is a standard angle-and-range traek with no ehirp transmission.

By selecting the display funetion every eighth pulse will receive narrow band ehirp using the pulse compression network. This allows a "look-ahead" to determine if the range error is small enough to eapture the target in 2.5 MHz chirp. When the 2.5 MHz mode is enabled the system interlaces one pulse CW for angle tracking and one pulse 2.5 MHz for range traeking. When the look ahead display is enabled in this mode every eighth pulse is ehirped to 5 MHz. A variable range bias can be preset to eorreet for timing and transition errors and afford a high probability of acquisition as the eompression is inereased from 2.5 to 5 MHz.

This proeess eontinues through 50 and 500 MHz until the system is interleaving CW and 500 MHz ehirp bandwidth. The effective range resolution obtained is also shown in Figure 3.3 for each compression bandwidth.

3.1.2.2 Test Mode. The test mode was extensively developed during this program to provide a rapid eheekout and systems ealibration facility using the PDP1 eomputer. This system would also be applieable to any other suitable computer system such as a Sigma 5.

Figure 3.4 is ineluded for referenee purposes and shows the effeetive range weighting for each range bit that ean be entered for test purposes using the range test facility on Cabinet 30, loeated downstairs.

Figure 3.5 shows the eontrol word formats from the PDP1 that enable the various eommands listed to be performed either manually or under program eontrol. These tests were assembled in a logieal pattern to exereise the system under program eontrol and are shown in Figure 3.6. Where these ealled for a repeated set of what were virtually subroutines, these are identified as Sequenee A Closed-Loop Tests as deseribed in Figure 3.7.

3.1.3 Hardware Assemblies. Most of the hardware rearrangement was eoneentrated in four eabinets, two downstairs (33 and 31) and two mounted on the antenna (77 in the PA/receiver room and 74 in the new room).

The only significant item not shown is the Synehronizer whieh is loeated in cabinet 30.

Figures 3.8 through 3.11 illustrate the equipment locations in the various racks.

MODE	FUNCTION	INTERLACE			RANGE GATE	TRANSMIT MODE	PULSE B/W	RANGE RESOLUTION
		NB/WB	DISPLAY	NB/WB/DI				
ACQ 1	ACQUIRE TARGET	N/A	N/A	N/A	250 μs	CW	25 KHz	20,000 FT
ACQ 2	UPDATE RANGE & ANGLE TRACKERS	N/A	1/1	N/A	250 μs	CW	25 KHz	20,000 FT
2.5	UPDATE RANGE TRACKER	1/1	1/8	1/1/8	40 μs	CHIRP	2.5 MHz	200 FT
5.0	UPDATE RANGE TRACKER	1/1	1/8	1/1/8	20 μs	CHIRP	5.0 MHz	100 FT
50.0	UPDATE RANGE TRACKER	1/1	1/8	1/1/8	2 μs	CHIRP	50.0 MHz	10 FT
500.0	DATA MODE	1/1	N/A	N/A	200 ns	CHIRP	500.0 MHz	1 FT

Figure 3.3 Acquisition Modes

BIT	MICROSECONDS	FEET	KILOMETERS
0	0.000390625	.194	0.00005
1	0.00078125	.388	0.000103
2	0.001562	.776	0.000236
3	0.003125	1.552	0.000473
4	0.00625	3.104	0.0009461
5	0.0125	6.208	0.0018922
6	0.025	12.416	0.0037844
7	0.05	24.832	0.0075688
8	0.1	49.664	0.0151376
9	0.2	99.328	0.0302752
10	0.4	198.656	0.0605503
11	0.8	397.312	0.121101
12	1.6	794.624	0.242201
13	3.2	1589.248	0.484403
14	6.4	3178.496	0.968806
15	12.8	6356.992	1.937611
16	25.6	12713.984	3.875222
17	51.2	25427.968	7.750445
18	102.4	50855.936	15.500889
19	204.8	101711.872	31.00178
20	409.6	203423.744	62.00356
21	819.2	406847.488	124.00711
22	1638.2	813795.976	248.04501
23	3276.4	1627591.952	496.09003
24	6552.8	3255183.904	992.18005

Figure 3.4 Bit Values for the 5K Register

TEST ADDRESS

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}	2^{17}	
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Reset Attenuation
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Reset Frequency
1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	45 MHz Test Cmd ON
1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	45 MHz Test Cmd OFF
1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	950 MHz Test Cmd ON
1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	950 MHz Test Cmd OFF
1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Noise Source ON
1	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	Noise Source OFF
1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	3.35 GHz Test Cmd ON
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	3.35 GHz Test Cmd OFF
1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	Waveguide Correction Test Cmd ON
1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	Waveguide Correction Test Cmd OFF
1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Noise Test Cmd ON
1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Noise Test Cmd OFF
1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Waveguide Switch Cmd ON
1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Waveguide Switch Cmd OFF
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	Vertical 32 db Test Cmd ON
1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	Vertical 32 db Test Cmd OFF
1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	Horizontal 32 db Test Cmd ON
1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	Horizontal 32 db Test Cmd OFF
1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	System Test ON
1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	System Test OFF
1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0 db Attenuation
1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	6 db Attenuation
1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	12 db Attenuation
1	1	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	18 db Attenuation
1	1	0	0	1	0	0	0	1	0	1	1	0	0	0	0	0	0	24 db Attenuation
1	1	0	1	1	0	0	0	1	1	1	1	0	0	0	0	0	0	30 db Attenuation
1	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	36 db Attenuation
1	1	0	1	0	1	0	0	1	0	1	0	1	0	0	0	0	0	42 db Attenuation
1	1	0	0	1	1	0	0	1	0	0	1	1	0	0	0	0	0	48 db Attenuation
1	1	0	1	1	1	0	0	1	1	0	1	1	0	0	0	0	0	54 db Attenuation
1	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	60 db Attenuation
1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	25 MHz
1	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	25.111 MHz
1	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	24.111 MHz
			MHZ			100 KHZ				10 KHZ				1 KHZ				

Frequency is in BCD

Figure 3.5 Test Control Words

TEST

1. Address System Test "ON".
2. Address Noise Source "ON".
3. Address Waveguide Switch CMD "ON".
4. Address Noise Test CMD "ON".
5. Set AGC Controls to "AUTO".
6. Start D.H.E.
7. Run Sequence "A1".
8. Address Noise Test CMD "OFF".
9. Address Noise Source "OFF".
10. Address 45 MHz Test CMD "ON".
11. Run Sequence A1 - A11.
12. Address 45 MHz Test CMD "OFF".
13. Address 950 MHz Test CMD "ON".
14. Run Sequence A1-A11.
15. Address 950 MHz Test CMD "OFF".
16. Address 3.35 GHz Test CMD "ON".
17. Run Sequence A1-A11.
18. Address +32 db VERT "ON".
19. Address +32 db HORIZ "ON".
20. Run Sequence A-1.
21. Address +32 db VERT "OFF".
22. Address +32 db HORIZ "OFF".
23. Run Sequence A-1.
24. Address Waveguide CORR CMD "OFF".

Figure 3.6 Test Sequence

25. Run Sequence A1-All.
26. Address Waveguide CORR CMD "OFF".
27. Stop DHE.
28. Set AGC to MAN (MAX ATTN).
29. Start DHE.
30. Repeat Steps 12 - 26.
31. Address System Test "OFF".
32. Reset FREQUENCY.
33. Reset ATTENUATION.

TEST COMPLETE.

Figure 3.6 Test Sequence (continued)

1. Set ATTENUATION to "0" db, and FREQUENCY to 23.776 MHz and SWEEP FREQUENCY in 36 KHz steps from 23.776 MHz to 26.224 MHz.

2. Set ATTENUATION to "6" db and SWEEP FREQUENCY in 36 KHz steps from 26.224 MHz to 23.776 MHz.

3. Set ATTENUATION to "12" db and SWEEP FREQUENCY in 36 KHz steps from 23.776 MHz to 26.224 MHz.

4. Set ATTENUATION to "18" db and SWEEP FREQUENCY in 36 KHz steps from 26.224 MHz to 23.776 MHz.

5. Set ATTENUATION to 24 db and SWEEP FREQUENCY in 36 KHz steps from 23.776 MHz to 26.224 MHz.

6. Set ATTENUATION to 30 db and SWEEP FREQUENCY in 36 KHz steps from 26.224 MHz to 23.776 MHz.

7. Set ATTENUATION to 36 db and STEP FREQUENCY in 36 KHz steps from 23.776 MHz to 26.224 MHz.

8. Set ATTENUATION to 42 db and STEP FREQUENCY in 36 KHz steps from 26.224 MHz to 23.776 MHz.

9. Set ATTENUATION to 48 db and STEP FREQUENCY in 36 KHz steps from 23.776 MHz to 26.224 MHz.

10. Set ATTENUATION to 54 db and STEP FREQUENCY in 36 KHz steps from 26.224 MHz to 23.776 MHz.

11. Set ATTENUATION to 60 db and STEP FREQUENCY in 36 KHz steps from 23.776 MHz to 26.224 MHz.

Figure 3.7 Sequence "A" - Closed Loop Test

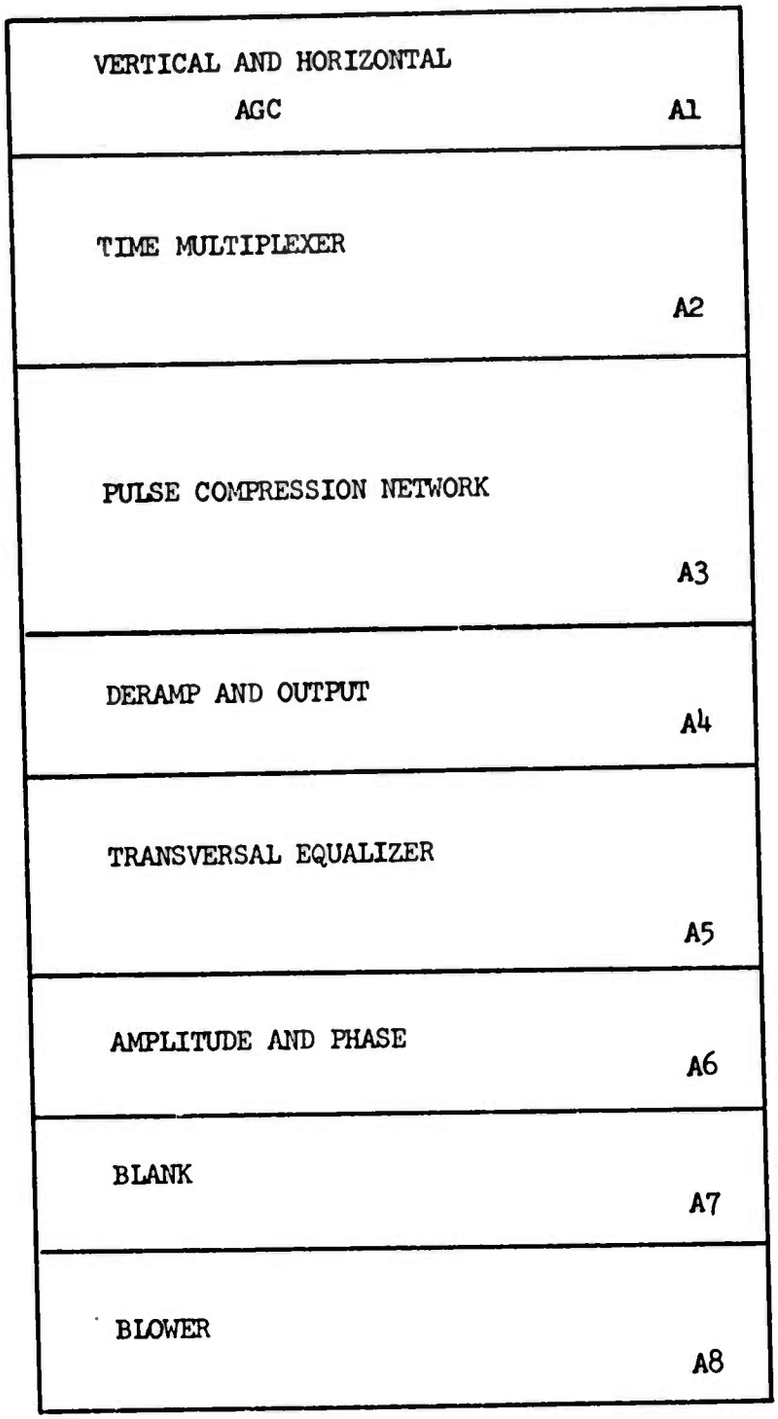


Figure 3.8 Wideband Compression Cabinet - Unit 23

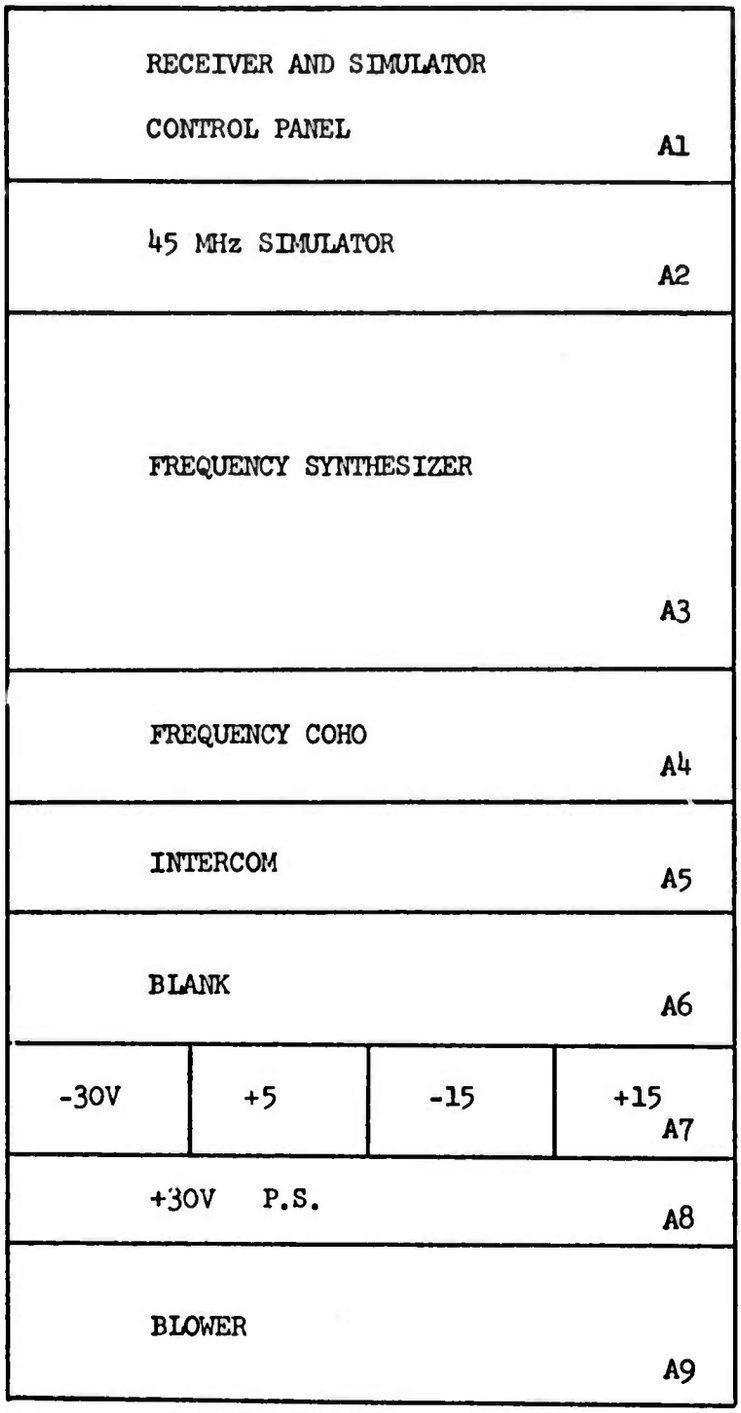


Figure 3.9 Unit 31 Layout

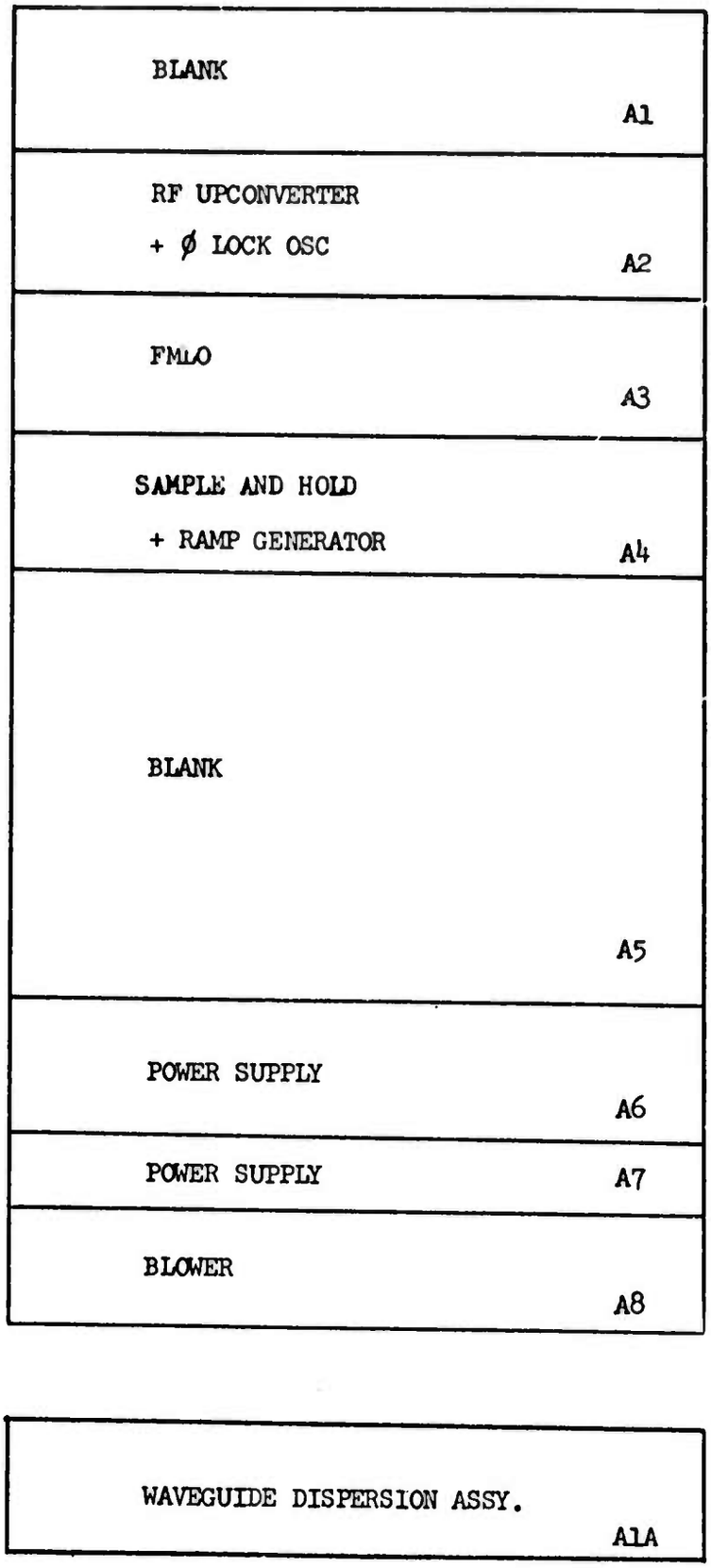


Figure 3.10 Exciter Cabinet - Unit 74

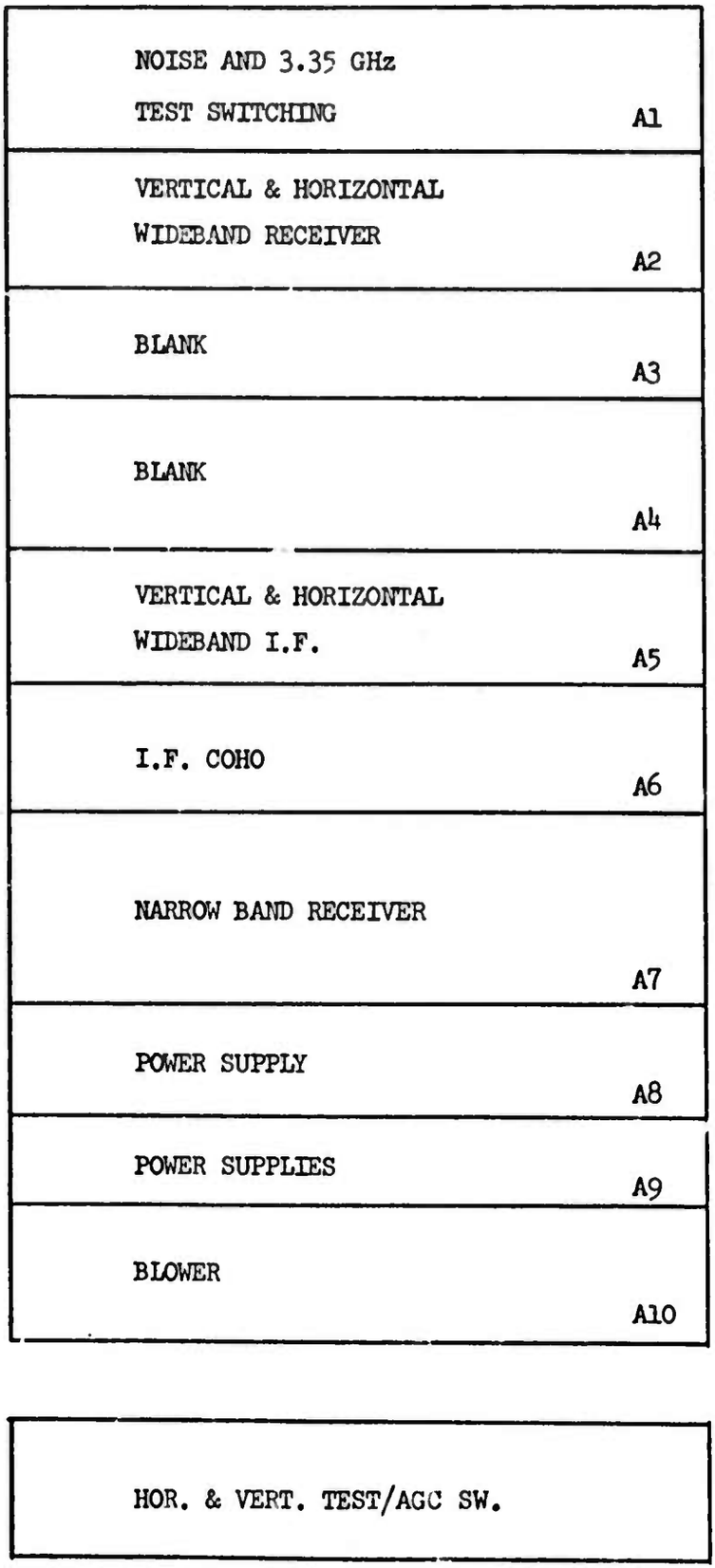


Figure 3.11 Unit 77 Layout

3.2 Wideband Sweeper.

3.2.1 RF Subsystem.

General Description. A block diagram of the wideband sweeper subsystem as finally implemented appears in Figure 3.12. The VCO is driven by the voltage ramp generator which generates a linear sawtooth and sums it with a sampled passive correction signal to provide an ultra-linear frequency/voltage characteristic out of the voltage controlled oscillator.

During the time the VCO is not sweeping, a phase-lock error signal, derived by comparing the VCO output with a 2.4 GHz reference signal, is fed to the voltage ramp generator for processing and scaling before being applied to the VCO varactor terminals.

Monitoring means are provided for determining that the VCO is locked in phase, time-sidelobe performance, and the presence of the 2.4 GHz reference signal.

The wideband sweeper is capable of producing waveforms of three different bandwidths, namely 5 MHz, 50 MHz, and 500 MHz as well as CW operation for acquisition.

Phase Lock Mode. The driving signal for the VCO in the non-sweeping or phase-lock mode is derived as follows: A sample of the VCO output is taken thru a 10 db directional coupler and fed to the "R" port of a Watkins-Johnson double-balanced mixer operated as a phase detector. Likewise, a sample of the 2.4 GHz is fed thru a SPST solid-state high speed switch to the "L" port of the same mixer. The output of the mixer at Port "X" is proportional to the cosine of the angle between the two signals, thus:

$$V_{out} = A \times B \cos \theta$$

Where A and B are the two input signals whose amplitude is held constant by driving the mixer to the point of saturation, and θ is the phase angle between A and B.

Sufficient attenuation is added to the path between the phase detector output and the ramp generator input to provide the correct gain constant for a stable loop operation, and to provide an isolated path for monitoring purposes.

Just prior to the initiation of the sweep mode, the SPST switch is opened up, allowing the VCO to be driven to the high end of the band at the application of the sawtooth.

Sweeping or Chirp Mode. In the test facility radar the transmitted signal in the data mode is a down-chirped FM waveform of three possible bandwidths, 5 MHz, 50MHz or 500 MHz, each 40 microseconds in duration.

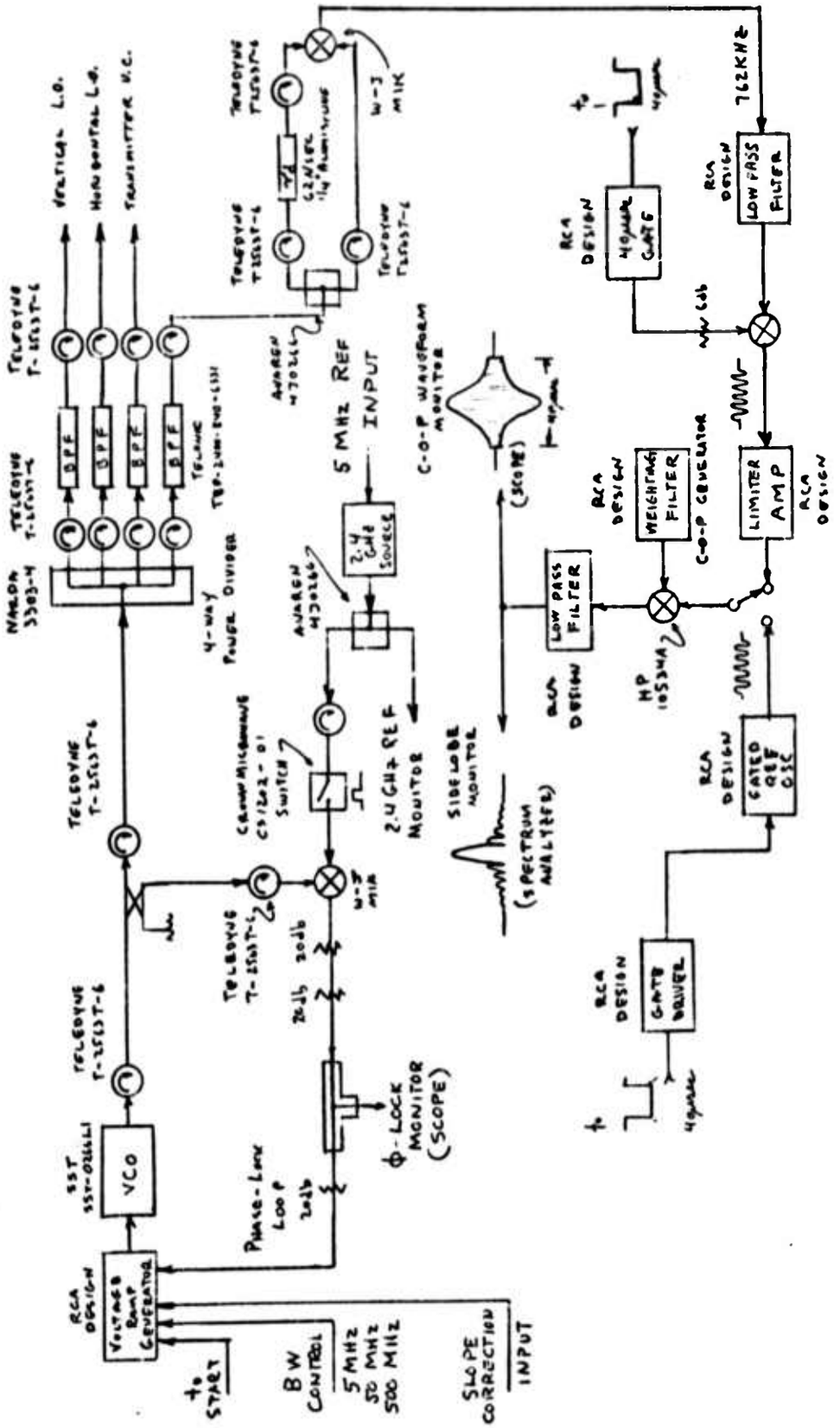


Figure 3.12 Wideband Waveform Generator Block Diagram

In order to optimize the linear output of the sweeper, the varactor is driven by a greater voltage swing than is utilized, namely 42 microseconds, the output being subsequently gated further in the system by a 40 microsecond gate in the upconverters and downconverters.

As can be seen from Figure 2.7 the frequency/voltage characteristic of the voltage oscillator deviates from a perfectly straight line by less than 1%. However, this is not sufficiently linear to produce time sidelobes in the 30-40 db area, particularly when the target of interest is displaced from the center of the range window.

Thus it is necessary to improve the linearity even further than that achieved by passive computerized linearization techniques presently available.

This is accomplished in the RADC SOI Test Facility sweeper by summing a series of 50 voltage steps, each 800 nanoseconds wide, and adjusted in level so as to compensate for VCO nonlinearity at a particular point in time.

The stepped curve in Figure 2.7 labeled "Passive Slope Correction" is the calculated correction derived from the actual voltage/frequency characteristic of the VCO. The photographs in Figure 3.13 show the actual 50 voltage steps applied to the VCO in open-loop fashion along with the summed output of the voltage ramp generator. The rather close correlation of the computed correction with the actual correction inserted into the VCO can be seen by comparison of these two pieces of data.

The net result was an achievement of 25 db time sidelobes of the transmitted waveform when observed as noted on the block diagram of the sweeper. Photographs of two waveforms are shown in Figure 3.14. The top one is the spectral response of the weighted output of a gated reference oscillator tuned to the same frequency as that obtained by comparing the chirp waveform with a replica of itself delayed by 62 nanoseconds.

The weighting function was a cosine-on-a-pedestal and is shown in the lower photograph. This function is far from ideal due to hardware limitations imposed by budgetary considerations. Thus even the relatively pure output of the gated reference oscillator has sidelobes about 27 db down, whereas the beat frequency, f_b, from the sweeper shows worst-case sidelobes about 25 db down, without the normal taper characteristics associated with the far out sidelobes.

3.2.2 System Accuracy Requirements. Before further discussion on the sweeper is continued, it is deemed pertinent at this point to discuss some of the accuracy requirements for the wideband sweep generator used at the test facility.

The useful functioning of the test facility wideband signal processing approach relies on two fundamental facts: 1) interest is limited to targets appearing in a 100 foot (30 meter) range window, and 2) the target of interest is in precision range track.

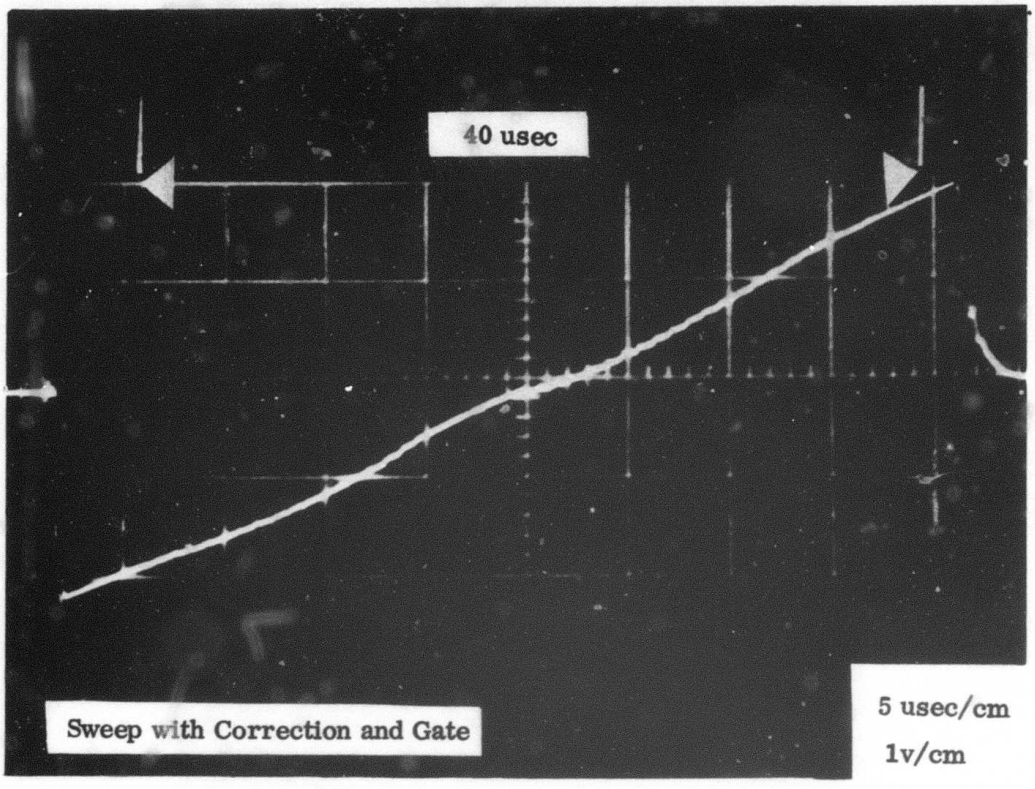
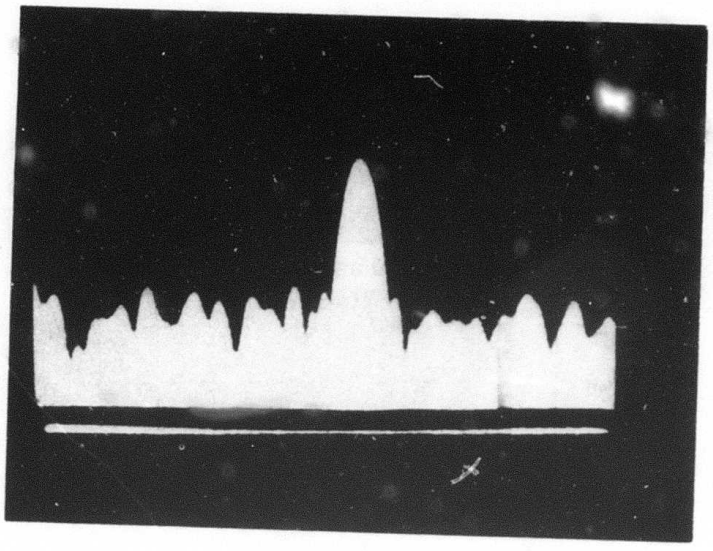
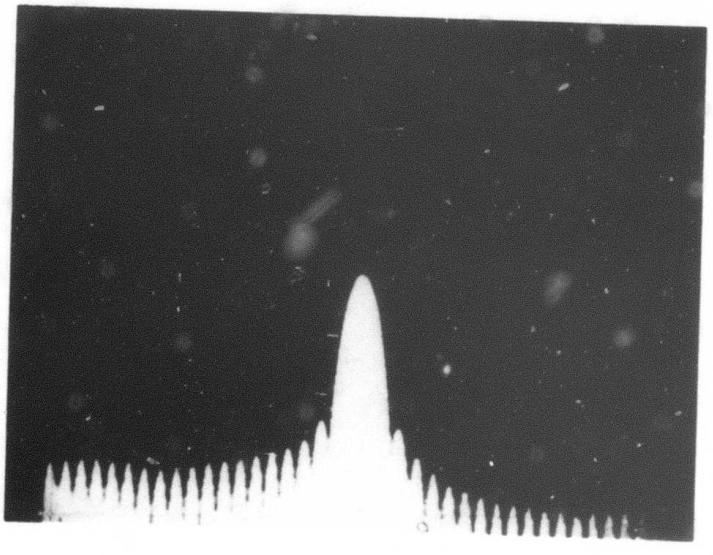


Figure 3.13 VCO Waveform



VCO Spectrum



Gated Sine Wave Spectrum

Figure 3.14 VCO and Gated Sine Wave Spectra

The 100-foot range window is divided into 100 range cells, each representing 2 nanoseconds of range (time) resolution. Range (time) resolution corresponds to the inverse of the RF swept bandwidth of the target return ($\frac{1}{500}$ MHz = 2 nanoseconds). The corresponding spectral width is the reciprocal of the uncompressed pulse ($\frac{1}{40 \text{ usec}}$ = 25 KHz). Thus each range cell represents a frequency increment of 25 KHz.

Figures 3.15 and 3.16 illustrate the principle of operation of the Floyd Site Radar Bandwidth compression method. At transmit time, the FMLO produces a linear frequency ramp having a center frequency of 2400 megahertz, an excursion of 497.5 megahertz and a time duration of 40 microseconds. This signal is then mixed with another signal centered at 950 MHz and a frequency excursion of 2.5 MHz, amplified and radiated toward the target as RF energy at f_o = 3.35 GHz.

At echo-receive time (as predicted by a precision range tracker) the FMLO is again triggered, producing a reference or correlation ramp identical to the transmit ramp, but offset from it by the first IF, 950 MHz. The reference ramp (f_o = 2.4 GHz) is applied to the local oscillator port of the correlation mixer. The received target echo ramp is applied to the signal port of the correlation mixer. The output of the correlation mixer is a 40 microsecond wide pulsed sinusoid having a center frequency of 950 MHz and a frequency excursion of $\pm$1.25 MHz. This is shown as waveform B in Figure 3.16.

As an example, let us consider a target 15 meters closer or farther in range than that which produced time-coincident signal and reference ramps. This target will generate an echo ramp displaced in time by $\pm$100 nanoseconds with respect to the reference ramp. Because both ramps have a slope = 12.5 MHz/usec (12.4375 MHz/usec for the reference ramp), the $\pm$ nanosecond time (or range) offset produces a corresponding frequency offset of $\pm$1.25 MHz in the center frequency of the signal at the correlation mixer output. The sign of the 1.25 MHz offset is dependent on the direction of the range offset.

Thus, the correlation process translates differences in target range into differences in frequency within the pulsed ramps at the correlation mixer output. Targets in the range window separated by 1/3 meter (2 nanoseconds) produce pulsed ramps whose center frequencies differ by 25 KHz. This can be seen in Figure 3.16 by comparing waveform A&C with waveform B. The nominal range resolution (1/3 meter) inherent in the 500 megahertz bandwidth signal is thus preserved in the form of frequency separation between 40 microsecond pulses. (Note that the spectral width of a 40 usec pulse is 25 KHz). The frequency/time conversion factor is 12.5 KHz/nsec.

It should be noted that although the bandwidth of any one target signal at the correlation mixer output is only 25 KHz, the composite of signals distributed across the 30 meter range window occupies a band of frequencies distributed across a 2.5 MHz band centered at the IF. Therefore all components following the correlation mixer must process the signals covering the 2.5 MHz band without distortion.

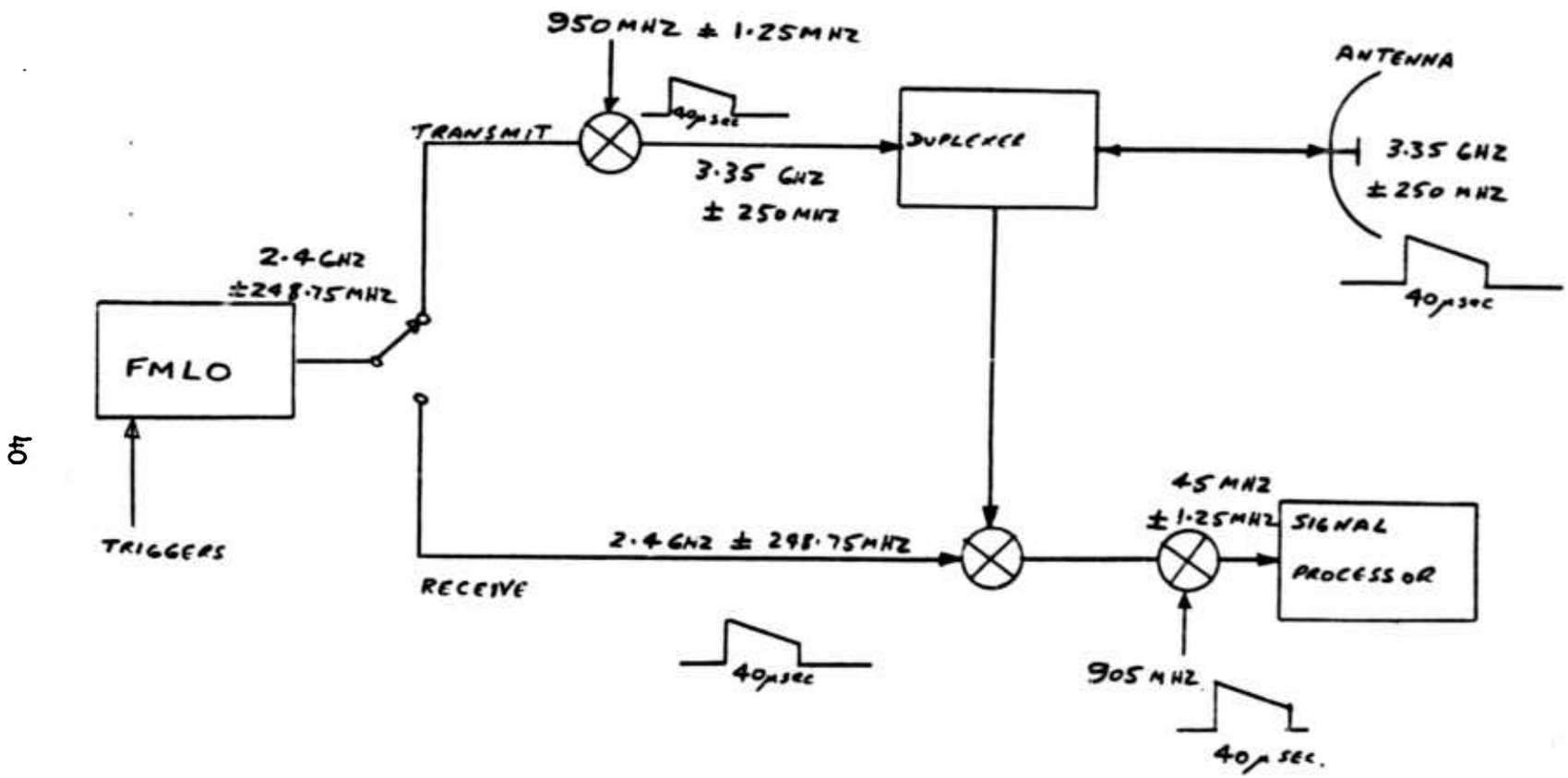


Figure 3.15 Test Facility Radar Bandwidth Compression Scheme

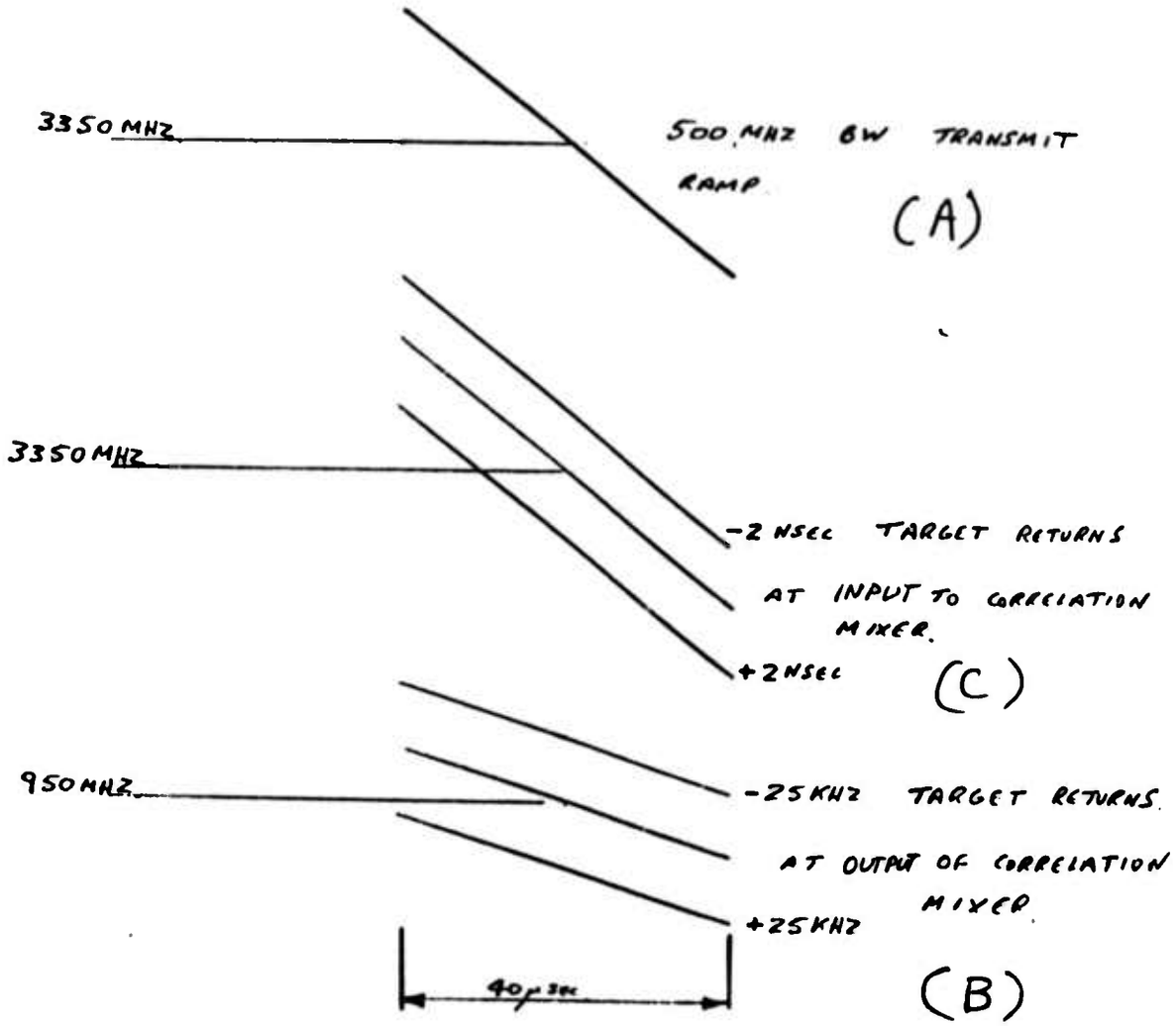


Figure 3.16 Signals at Mixer Ports

Now then, in view of the above, let us consider the accuracy with which successive ramps must be reproduced. Figure 3.17 illustrates a typical case of wideband target return in one of the range cells. In the wideband mode of operation, the range tracker operates in the centroid mode; that is, the position of the range gate is maintained on the electrical center of gravity of the target.

If the frequency of a successive ramp differs from the previous by $\pm$25 KHz the target will jump into an adjacent range cell; hence the energy in the cell where the range gate is centered will be very low, resulting in a range jitter and eventual loss of track. A reasonable tolerance on frequency repeatability would be about a third of a range cell or $\pm$8 KHz.

Looking at the problem from another viewpoint, that is, the timing of the generation of successively ramped pulses. What is critical here is the time between the impulse trigger and the time when the useful sweep occurs.

As seen in the earlier discussion Figure 3.16 shows the effect of return echoes occurring at +2 nanoseconds and -2 nanoseconds with respect to a correctly centered ramp. At RF, the two nanoseconds represents one range cell, and any deviation in timing will again result in a range jitter. The tolerance specified for the FMLO sweeper is $\pm$0.39 nanoseconds, which is somewhat less than one-fifth of a range cell.

This may seem unnecessarily stringent in view of the one-third range cell constraint on frequency. However, in this case, the tolerance on the generation of the impulse itself is $\pm$0.2 nanoseconds. Thus the composite peak to peak time jitter is $\pm$.59 nanoseconds, which is close to one-third of a range cell. This, in addition to the frequency tolerance of one-third range cell places a burden on the range tracker presently employed.

The above calculations were made considering peak-to-peak jitter; the RMS jitter would be stated as:

$$\text{Jitter}_{(\text{RMS})} = \sqrt{(0.39)^2 + (0.2)^2 + (.64)^2} = 0.78 \text{ nsec RMS}$$

The RMS jitter then extends to slightly more than one-third of a range cell and emphasizes the need for taking extra precautions in eliminating all sources of instability. Thus, the entire sweeper, power supplies, logic boards, etc. are mounted in an EMI-proof enclosure with filtered connectors, and the impulse signal is fed to the "upstairs" electronics by way of a double-shielded, twin-lead cable.

Phase jitter is measured as shown in Figure 3.18.

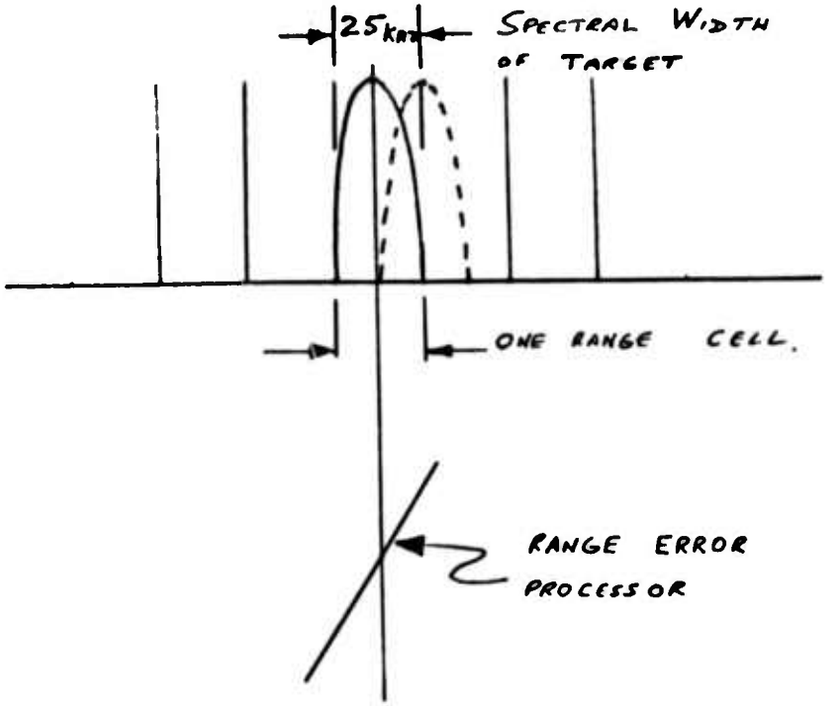


Figure 3.17 Frequency Stability Effects

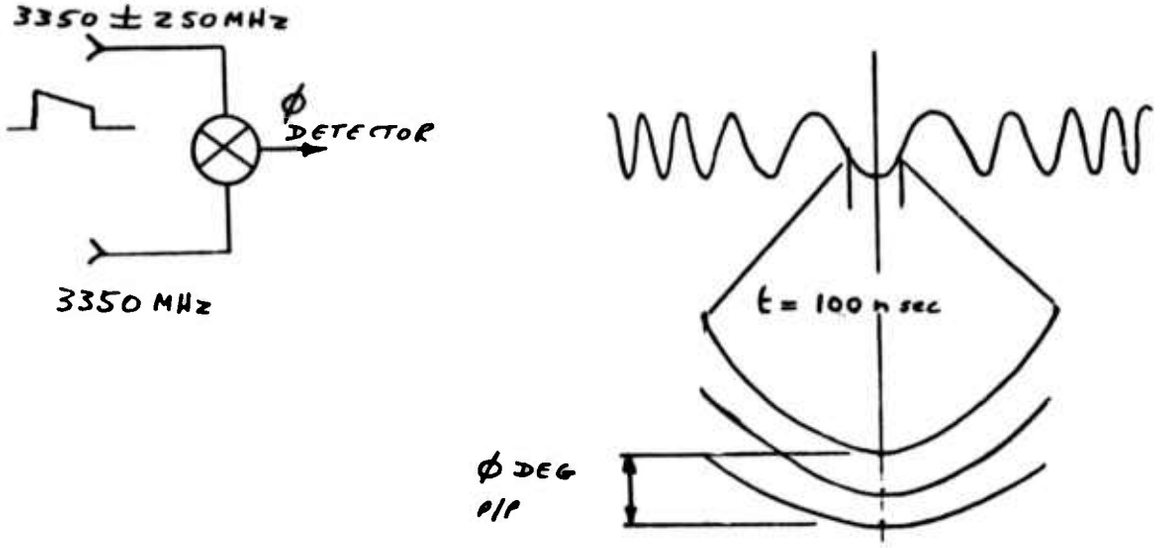


Figure 3.18 Phase Jitter Measurement

Returning to the Block Diagram of the Wideband Waveform Generator, Figure 3.12, it can be seen that a sample of the VCO output is taken by means of a four-way power divider and fed to a three db hybrid. One leg of the hybrid is connected directly to the "L" front of a Watkins-Johnson Model MIK mixer, while the other output of the hybrid is connected thru a 62 nanosecond delay line to the "R" front of the mixer. The output at the "X" Port of the mixer represents a beat frequency between the two ramps as follows:

$$f_b = \frac{BW}{T} \cdot \tau \qquad (1)$$

where BW is the 500 MHz swept bandwidth of the system; T is the pulse width, 40 microseconds; and τ is the time delay presented by the delay line.

The output frequency, then, is

$$f_b = \frac{500 \times 10^6}{40 \times 10^{-6}} \times 61 \times 10^{-9}$$

$$= 762.5 \text{ KHz}$$

A photograph of the gated output of the f_b mixer prior to limiting is shown in Figure 3.19.

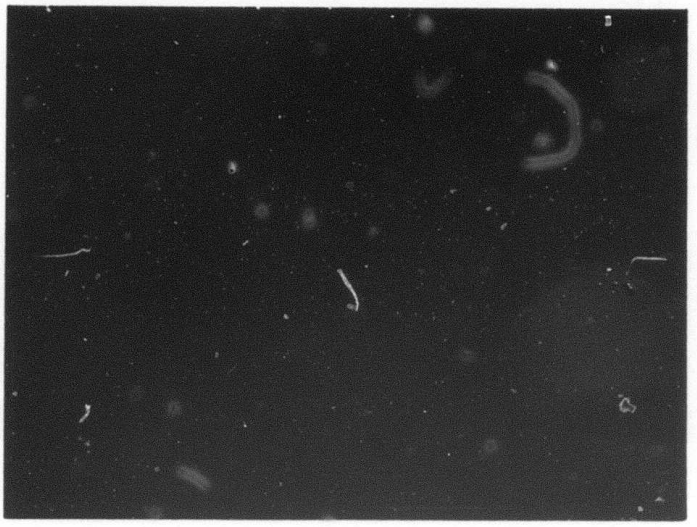
Coarse adjustment of the 50 voltage steps (sample-and-hold outputs) is accomplished by comparing this waveform with the output of the gated reference oscillator (tuned to 762.5 KHz) on an oscilloscope. The two waveforms are aligned so that the peaks are coincident at the start of the pulse, then each sample and hold element is adjusted until the f_b waveform is in exact coincidence with the gated oscillator output at every point in time along the pulse length.

The sample and hold adjustments can be made to an accuracy of ± 0.1 cycles or ± 36 degrees. This, of course, is inadequate as it would produce sidelobes near 10 db. Hence, a fine tuning alignment is accomplished by phase detecting the gated reference oscillator output and the beat frequency, f_b, resulting in a phase ripple of about two to three degrees, representing sidelobes in the order of 32 db. Figure 3.20 shows the VCO correction.

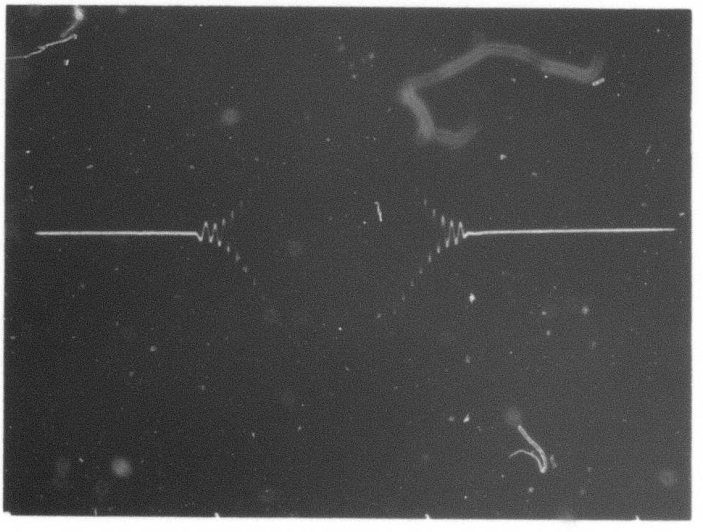
A delay line of 61 nanoseconds was used in this interim sweeper out of expediency. Had the program allowed the design of a true closed loop system, a longer delay would have been used based on the relationship developed by A. G. Cressanthis of RCA, Moorestown in the following fashion:

The phase function for a linear FM ramp with initial frequency $f_o = \omega_o / 2\pi$ is:

$$\phi(t) = \pi \frac{B}{T} t^2 + \omega_o t \qquad (1)$$

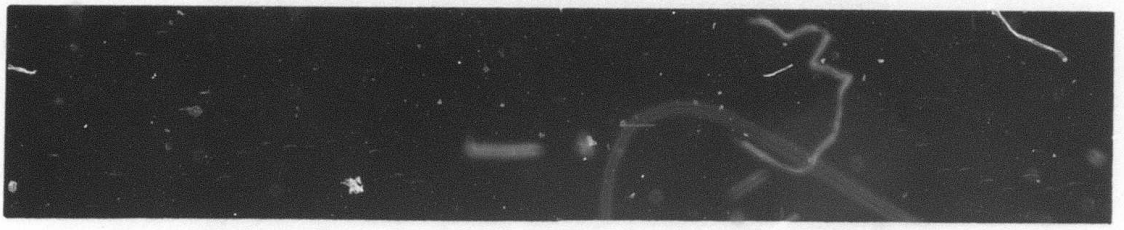


(a) Sweep Generator Mixer Output



(b) Cosine on Pedestal

Figure 3.19 Sweep Generator Mixer O/P and Cosine on Pedestal



2 usec/DIV & .2V/Div

5 usec/DIV & .2V/Div

Figure 3.20 Sample and Hold VCO Correction

The phase difference between the ramp and the ramp delayed by T is:

$$\phi_b = \pi \frac{B}{T} t^2 + \omega_o t - \left[\pi \frac{B}{T} (t - \gamma)^2 + \omega_o (t - \gamma)\right] \quad (2)$$

$$\phi_b = 2\pi \frac{B}{T} t\gamma - \frac{B}{T} \gamma^2 + \omega_o \gamma \quad (3)$$

if we define $\omega_b = \frac{d\phi_b}{d_t} = 2\pi \frac{B}{T} \gamma$

then $f_b = \frac{\omega_b}{2\pi} = \frac{B}{T} \gamma$

f_b is the beat frequency out of the mixer and the pulsed oscillator frequency.

f_r is selected to equal f_b.

Now consider the phase of the mixer output signal at the sampling times Ny; N=0, 1, 2, 3 - - - . This is simply the difference in phase between the delayed and undelayed ramp or the change in the ramp phase at times t = nY and t = (N+1)y.

Using (1)

$$\phi(n+1)\gamma - \phi(N)\gamma = \pi \frac{B}{T} (N+1)^2 \gamma^2 + \omega_o (N+1)\gamma - \pi \frac{B}{T} N^2 \gamma^2 - \omega_o N \gamma \quad (5)$$

$$\phi(N+1)\gamma - \phi(N)\gamma = \Delta\phi = 2\pi N \frac{B}{T} \gamma^2 + \pi \frac{B}{T} \gamma^2 + \omega_o \quad (6)$$

In order that the phase of the mixer output have a fixed relation to the phase of the reference for all sampling times, and to be consistent with the steady state operation of the loop with essentially zero error samples from the sampler, the following expression must be satisfied:

$$\Delta\phi = 2\pi n \quad (7)$$

Now from (6) and (7)

$$2\pi n = 2\pi N \frac{B}{T}\tau^2 + \pi\frac{B}{T}\tau^2 + w_o\tau$$

$$\text{or } n = N\frac{B}{T}\tau^2 + 1/2\,\frac{B}{T}\tau^2 + f_o\tau \qquad (8)$$

For (8) to be true for all values of N, $\frac{B}{T}\tau^2$ must be an integer.

If we consider the special case

$$\text{where } \frac{B}{T}\tau^2 = 1 \qquad (9)$$

$$\text{then } \tau^2 = \frac{T}{B} = \frac{40 \times 10^{-6}}{500 \times 10^{6}} = 8.00 \times 10^{-14}$$

$$\tau = 283 \times 10^{-9} = 283 \text{ nanoseconds} \qquad (10)$$

for the test facility parameters.

If the conditions in (8) are met, where n + N are integers, then the output ramp can only follow a family of ramps separated in frequency by $1/\tau$ and matching the phase function in (1) at least at times $n\tau$.

The beat frequency resulting from the use of this delay line would be

$$f_b = \frac{B}{T}\cdot\tau = \frac{500 \times 10^{6}}{40 \times 10^{6}} \quad 283 \times 10^{-9} = \underline{3.54 \text{ MHz}}$$

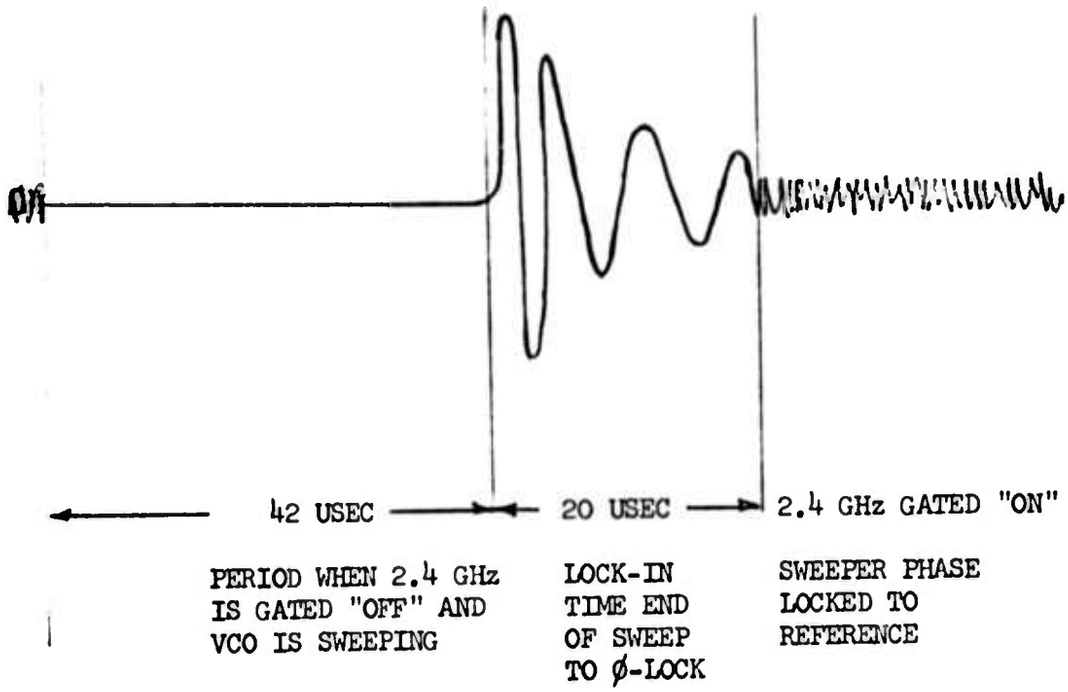
The advantage of this scheme of selection of the delay line is that ramp-to-ramp repeatability of the desired phase function is obtained despite noise on, or lack of perfect repeatability of, the drive waveform.

Figure 3.19b shows the result of applying the weighting function to either the gated reference oscillator output, or f_b as the case may be.

Preadjustment of the weighting filter is done by connecting the gated reference oscillator output into the weighting filter mixer and adjusting the level of modulating signal and DC pedestal simultaneously until the pedestal is 0.08 times the amplitude of the peak RF signal. This results in a modified Hamming weighting function.

Included in the Wideband Waveform Generator configuration are several monitors to assist in assessing performance as well as aiding the alignment of the unit.

The Phase Lock Monitor taps off a portion of the error signal in the phase lock loop for observation on the oscilloscope. A typical presentation appears below:



From the above sketch it can be noted that the VCO phase-lock loop has completely settled out after 20 usec and remains in tight phase lock until the error signal is removed and the voltage ramp is applied, causing the VCO to "downchirp" on command. This period could be reduced further by additional clamping of the sweep output period but the 20 usec period compares favorably with the TR recovery time.

3.2.3 Voltage Ramp Generator. The Voltage Ramp Generator schematic is shown in Figure 3.21. This unit is the third generation following initial units that were built to check out the VCO and phase locking system. The final unit utilizes the same basic architecture as the prototypes.

The VCO imposes very stringent requirements on the sweep generator due to its small voltage range (approximately 5 volts for 500 MHz swept), low input impedance (50Ω) and sweep repeatability. In addition the sweep start time must be rigorously controlled if the efforts to produce a low jitter trigger (20 p seconds) from the synchronizer are not to be jeopardized. Variable-sweep bandwidths are required for acquisition, and a fast lock up (about 20 u secs) is required from the phase lock loop to enable the sweeper to retirgger at short ranges for the receiver swept waveform. Extensive use of integrated circuit operational amplifiers and FET switches was made to satisfy these requirements.

In the quiescent stage, the gate 1 input is normally = 1, SW1 is enabled, and the phase locked loop is operating.

This supplies the phase detector input to the integrator I_2. Switch SW 4(2) is normally open and the integrator is operating. While observing the VCO spectrum for good spectral purity, potentiometer VR4 is used to control the integrator gain and the recovery time of the loop at the end of the sweep period. The output from the integrator is summed in a common summing amplifier I_3 which supplies unity voltage gain and linear power amplification necessary to drive the 50Ω input impedance of the VCO. Diode D_2 across the output limits any positive excursion which could damage the VCO. In the event that phase lock is lost following initial turn on the loop will not be locked and the integrator output from I_2 runs up towards +15V volts. This run up is detected by the difference amplifier I_4 after a 2 sec delay to prevent transient problems. The output of I_4 is normally below ground but rises rapidly to positive saturation. Diode D_1 conducts and SW4 operates. The contacts on SW2 reset the integrator I_2 and after the 2 sec delay SW4 releases. The system will now lock up and remain phase locked until the transmitter or receiver sweeps occur.

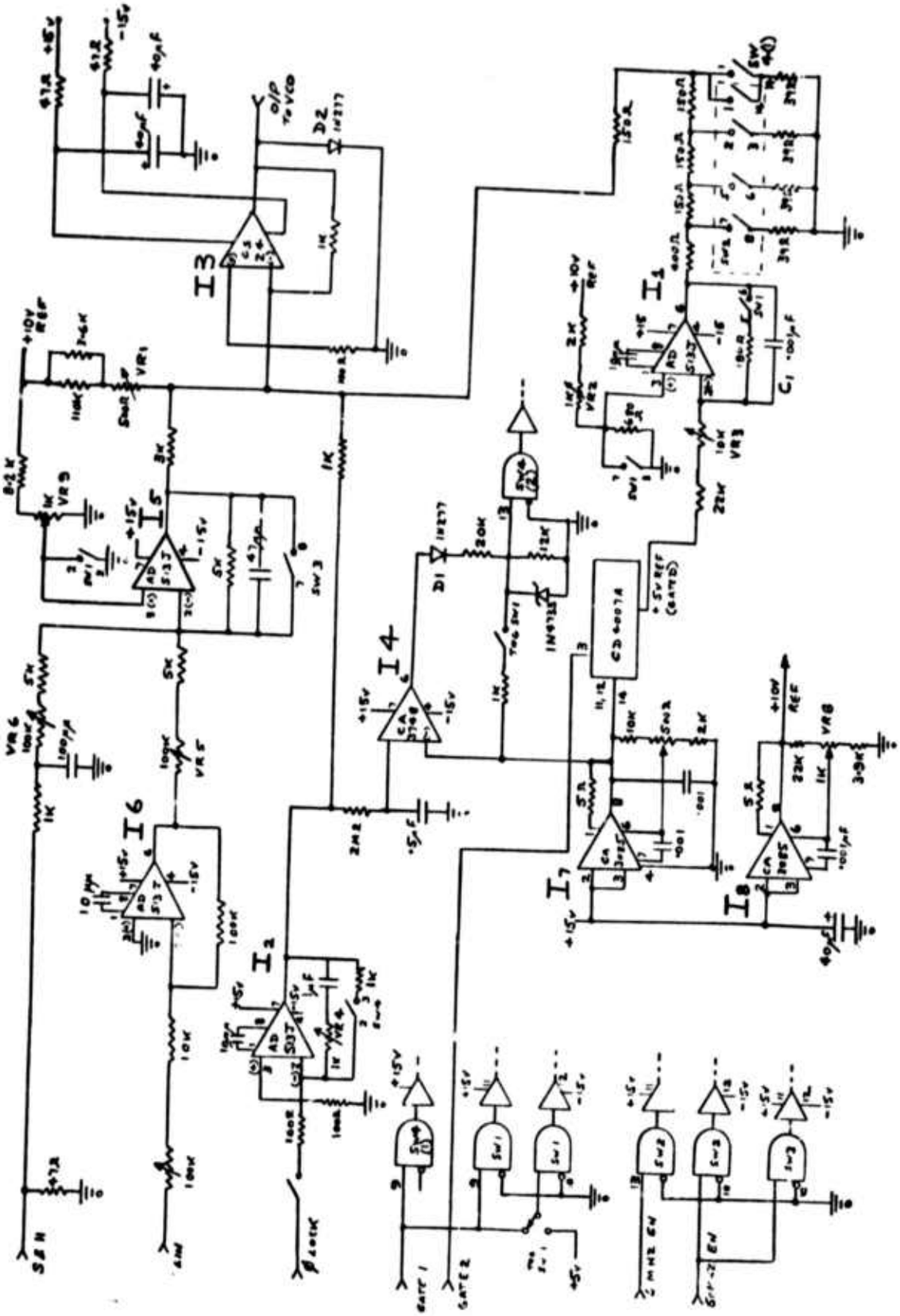


Figure 3.21 Voltage Ramp Generator

The VCO center frequency can be initially set to 2.4 GHz by VR1 but normally is set slightly below that to ensure phase lock capture as the integrator runs up prior to lock.

Toggle switch 1 is available to force a reset with SW 4, however, it should not normally be required except to confirm that the loop can be locked without the integrator.

The sweep is generated by integrator I_1 and requires a ramp that starts at approximately -4.8V and runs up to -.9 as shown in Figure 3.22. The initial VCO drop from center frequency is generated when gate 1 drops to 0. This drop causes SW 1 to open. I_1 receives a small positive voltage at the non inverting input which is inverted by the output stage I_3 and causes the output to drop and the VCO frequency to go to the high end (2.4 GHz + 250 MHz) prior to sweep generation. VR 2 allows the high frequency to be set to provide a 250 MHz deviation from center frequency. The phase lock is broken at the input to I_2 by SW 1 and the integrator stores the VCO voltage for rapid reacquisition at the end of the sweep period. Switch 1 opens releasing the clamp across the integrating capacitor C_1. The integrator is now coasting since no input has been applied to the +5V integrator reference line. About 1.6 usec after the application of gate 1 (sufficient time to allow the FET switch SW 1 to operate) the precision gate (FMLO gate) from the HI Speed Synchronizer is applied to the gate 2 input. This switches the internal reference +5 volts through a CD 4007A COS/MOS amplifier used as a precision fast rise time switch. The integrator now down-ramps and produces the inverted up-ramp at the O/P. The ramp slope is controlled by VR3.

At the end of the sweep period gates 1 and 2 terminate and the phase lock loop reacquires the VCO and returns it to 2.4 GHz in approximately 20 usecs.

Two additional analog input ports are provided on the sweeper. The S&H (sample and hold) is provided by a digital shift register technique. A 56 stage shift register selects one of 50 sample and hold circuits which have been preset to a voltage between 0 and +2. By choosing the correct clock frequency a new level can be selected for each 800 nsec across the 40 usec pulse. When correctly adjusted this predistortion function is used to linearize the small errors in the VCO output across the pulse. VR6 is used to provide an overall gain setting for the S&H level to I_5. Since the S&H signals are T^2L derived they are unipolar and can only provide a frequency deviation in one direction. VR9 and SW1 are used to provide a small depression of the base line during the sweep period. The sweep O/P with Sample and Holds added is shown in Figure 3.23.

Toggle SW1 is used to inhibit sweep generation and allow a measurement of the S&H levels across the pulse during initial alignment. The final setting of these controls is made by a frequency comparison technique and counting cycles across the pulse.

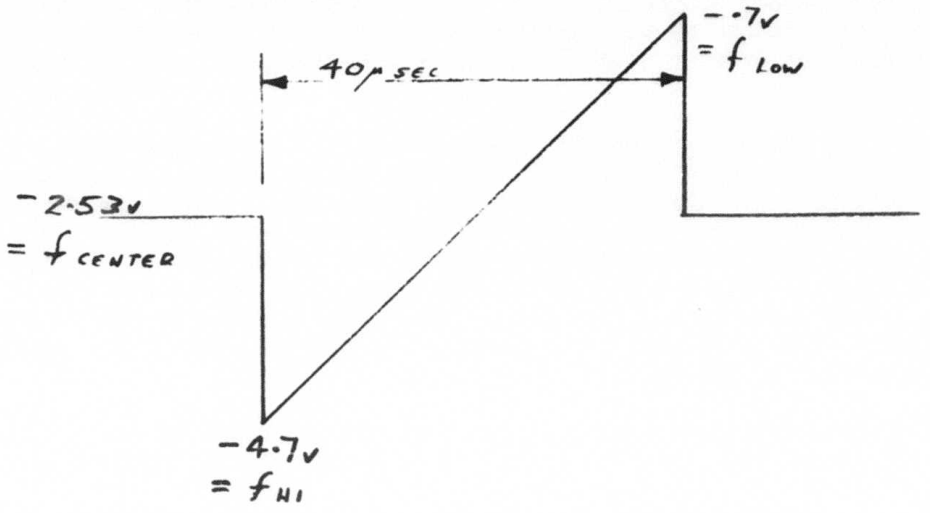


Figure 3.22 VCO Sweep Input

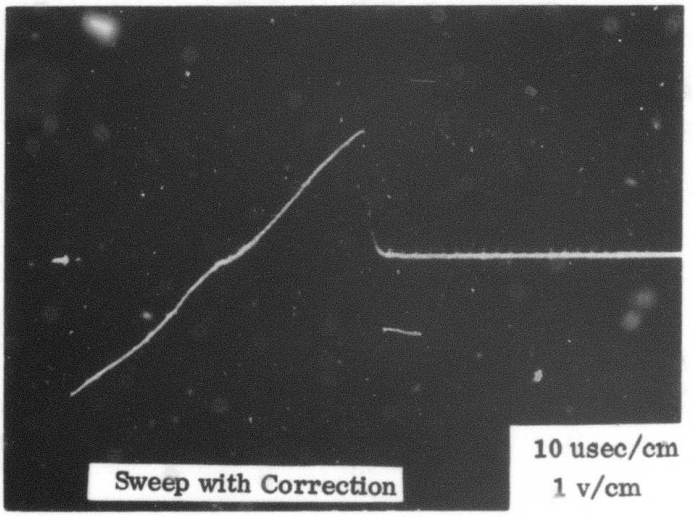


Figure 3.23 VCO Sweep with S&H Correction

An additional port for a linearity correction signal is available for dynamic correction across the pulse but was not used since good sidelobe performance was obtained by use of the S&H system alone. However, a possible future improvement would be to close the linearity loop and utilize the amplifier I_6.

In addition to the requirements described above the sweeper must generate 5 and 50 MHz sweeps during target acquisition. This is conveniently accomplished with a two stage ladder network controlled by SW2 which not only limits the sweep width but decreases the sweep excursion at the start of sweep, to maintain a constant center frequency for the sweep. The logic levels are normally set to 0 and all switches are open. Hence the output amplifier I_3 has unity gain. When the 50 MHz sweep is required the 50 MHz level is set to 1 closing half of the ladder network and providing a tenth of the output used at 500 MHz.

In addition, SW3 is enabled by this level and disables the S&H amplifier I_5 (since this input is not required during the acquisition period).

When the 5 MHz is required both the 5 and 50 MHz input are set to 1 enabling the complete ladder network and providing a hundred to 1 voltage attenuation. The additional contacts SW4(1) across the output of the ladder network is used to attenuate the transient that appears at this point during the discharge of C_1. This transient if unattenuated increases the recovery time of the phase lock loop to an undesirable 100 usec.

Two low current voltage regulators (I7 and I8) were included on this chassis to provide the necessary reference supplies that are free of load induced transients or noise pick up problems. It will be noted with the exception of the +5V to Tog SW1 all supplies are used to supply reference network voltages under virtually constant current conditions. For the case of the switch supply to SW1 this is only used to force a reset of phase lock integrator I_2 during initial alignment of the unit.

3.2.4 F Beat Limiter. The F Beat Limiter is required to provide an effective limiting function at approximately 1 MHz with signals as low as 5 mV p to p and over at least a 30 db range. In addition the output must be symmetrical about 0 under all signal level conditions and capable of driving at least 2 v p to p into a 50Ω load when driven with 40 usec wide pulses of RF at a PRF of 70/sec in a quasi pulse pair operation.

While the requirements seem almost mundane the ability to produce a symmetrical output about 0 with a very low mark to space ratio proved to be difficult to satisfy. Due to charging problems during the pulse the use of coupling capacitors was found to be unacceptable.

As a result of these problems the system shown in Figure 3.24 was developed to meet the limiter requirement.

The limiting function is performed by comparators I_1 and I_2. Diodes D1 and D2 are used to provide a few millivolts of offset voltage for each

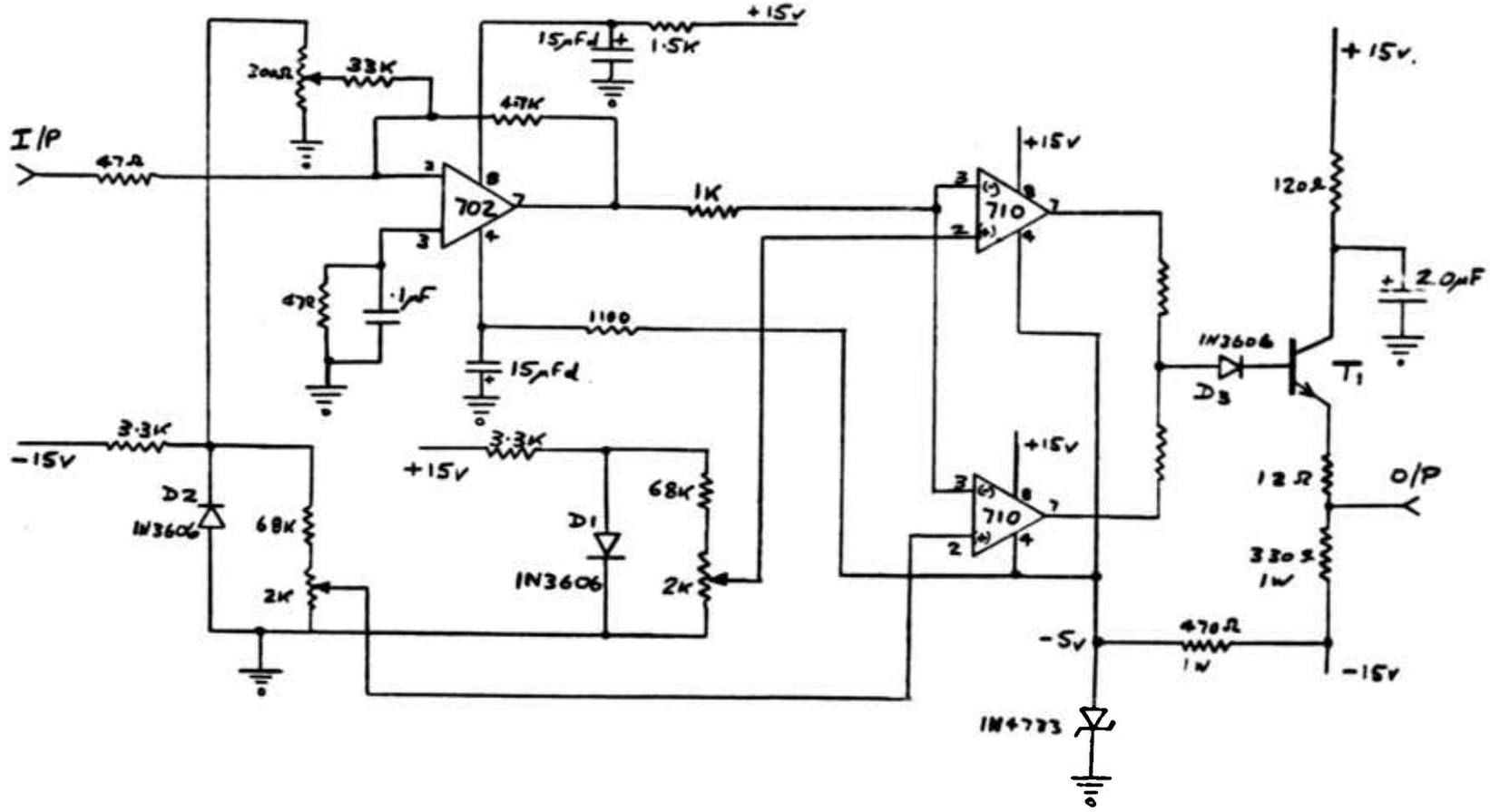


Figure 3.24 F Beat Limiter

comparator. The common input is very close to ground. The output from I_1 is equal to +3 volts while, due to the negative bias on I_2, the output from I_2 is at -.5 volts.

The output from the comparators is summed in the 4.7K output resistors and will normally be at +1.7 volts. As these input to the common input pin 3, moves cyclicly through the comparator area of input sensitivity, the output of each comparator will switch in turn, i.e., both comparators will either be on or off resulting in a square wave output that will vary between +3 and -.5 volts centered at +1.7 with no signal.

The 1.7 volt fixed bias is removed with the silicon diode D3. The output transistor T_1 is an emitter follower to provide the output power.

Amplifier I_3 is a X100 wideband amplifier to boost the low level signals prior to limiting. It is provided with a zero setting control to provide a true 0 at the common input of I_1 and I_2.

The performance curve Figure 3.25 was recorded under pulse drive conditions and shows the wide range and low level (approximately 5 mV) which can be applied to obtain the desired limiter characteristic.

3.3 Floyd Site Transmitter Upgrade

3.3.1 Introduction and Summary. This section of the report will cover the work performed in upgrading the performance, safety and operation of the SPTF Transmitter. Key pieces of data are presented and analyzed which demonstrate the best manner to operate the transmitter for the optimum phase and amplitude performance and at the same time identify the limitations imposed on the system by the transmitter with respect to time sidelobe performance.

Initial effort on the transmitter was devoted to accumulating data on the "as is" performance of the equipment, stage by stage, and also incorporating a number of safety provisions to facilitate the measurement program. The initial effort has been documented in an interim report (FOM 12) which is included in the appendix. A few key conclusions of the report are:

1. The bandpass characteristics of the transmitter were narrower then expected and contained greater than 3 db amplitude ripples and $\pm$50 degree phase ripple.

2. The Driver stage had insufficient output power across the band for good saturated operation of the final stage.

3. Refinements in phase measurement techniques were required although this would not change the gross conclusions reached.

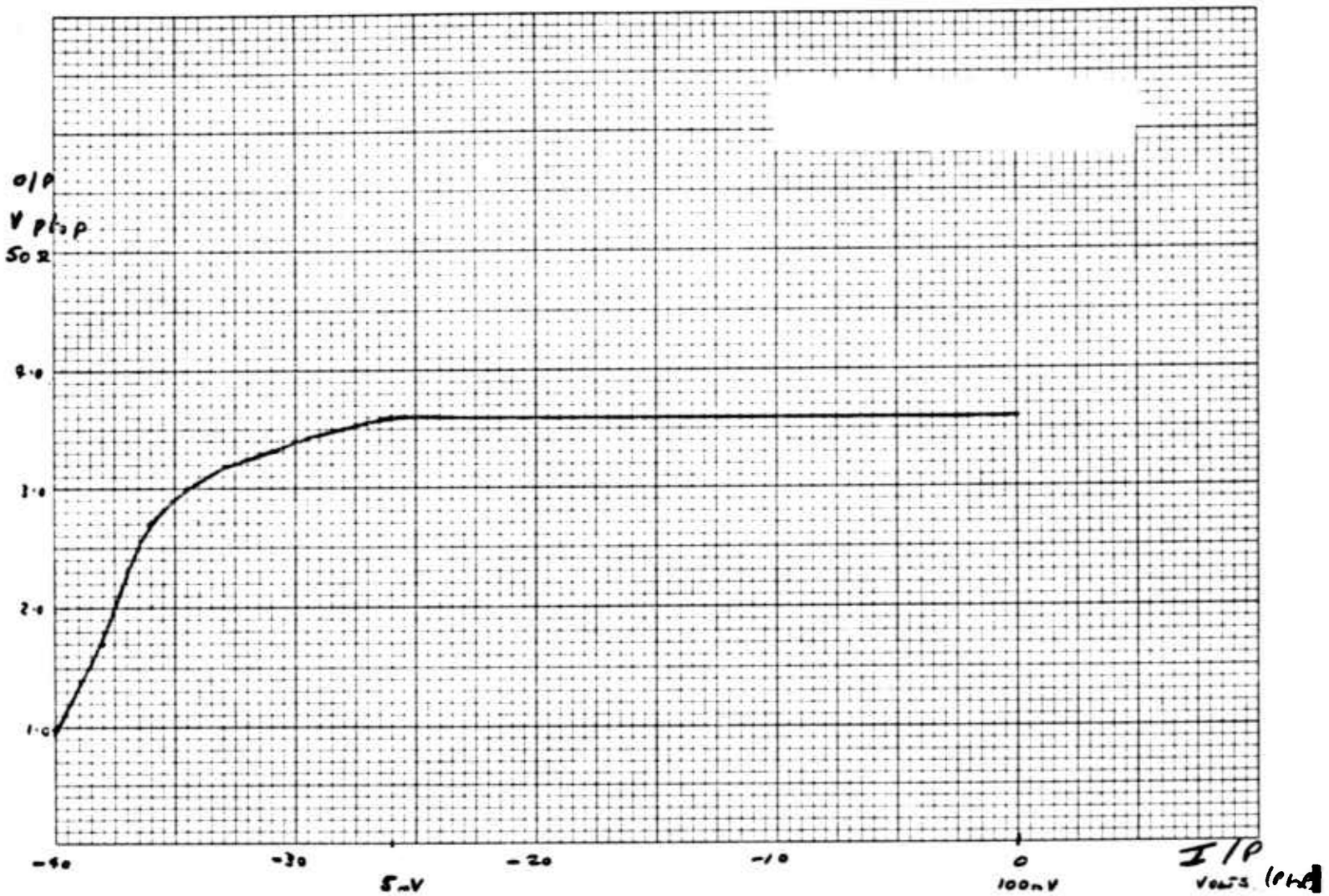


Figure 3.25 F Beat Limiter Characteristic

Based on these early results, a program was set up to refine the measurement techniques and accumulate fine grain phase and amplitude characteristics of the transmitter with the emphasis on determining and implementing changes in operation and in the equipment to realize improved performance.

The key results and detail conclusions of this program are contained in the following section. In summary, the data showed that the amplitude and phase performance is significantly improved by operating the Final Power Amplifier (FPA) at its full peak current rating and likewise setting the Focus Coil current as high as possible consistent with stable body current. On the order of 2:1 improvement in phase and amplitude performance was realizable by these changes. By themselves, these changes are insufficient to classify the transmitter performance as being good enough to support 35 to 40 db time sidelobes.

An effort was devoted to obtaining additional improvement in phase performance by utilizing the built-in "open" and "closed" loop phase compensation equipment. The open loop system was partially successful in that the phase ripple amplitudes could be reduced to a few degrees or to the minimum limits of the measurement set up. Its usefulness is, however, limited in practice by the criticality of the system control and stability which necessitates the need for continual control. This limitation was overcome by the closed loop phase control system. With the loop closed, phase ripple was reduced to the order of +10 degrees. Bandwidth stability limitations in the feedback loop prevented greater improvement. In general, more time and redesign effort is needed in this area to realize its full potential, but sufficient effort was expended to appreciate its usefulness as a phase correction technique.

The following section also presents performance data on the conversion of the transmitter from a 20 us, 250 MHz chirp system to a 40 us, 500 MHz chirp system.

Other significant tasks accomplished during the upgrade program were:

1. Inclusion of an SF-6 scrubber in the waveguide system with provisions to maintain the system under positive pressure during system off time.

2. Inclusion of a fault sensing system to provide fault isolation capability for collector current, body current, RF arc, and high VSWR faults.

3. Reconditioning most of the waveguide system to handle the significantly higher (20 - 24 KW) average powers achieved.

3.3.2 Performance Analysis.

3.3.2.1 Phase versus Frequency. Figures 3.26, 3.27 and 3.28 are slow frequency sweep graph data for the entire transmitter.

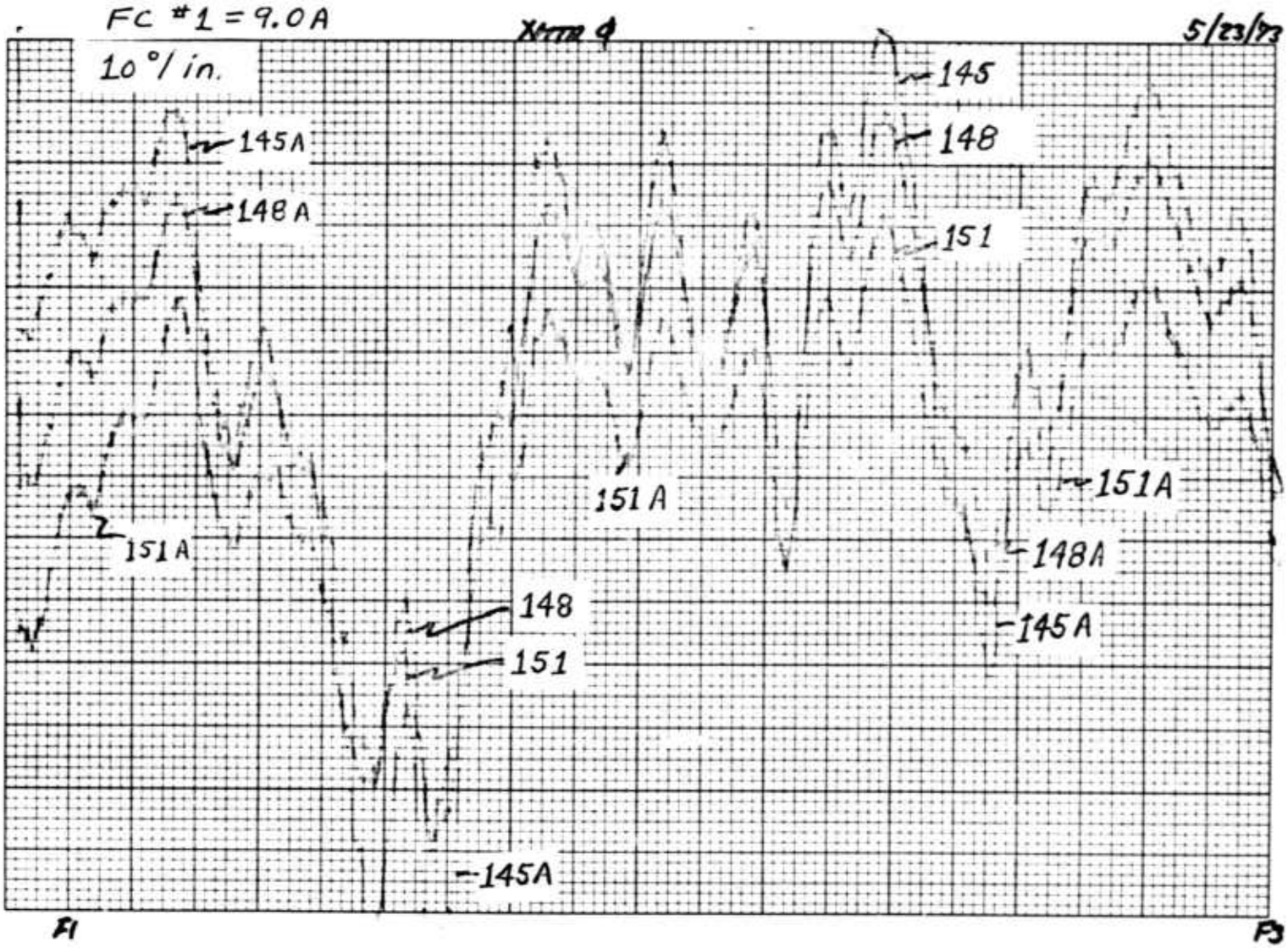


Figure 3.26 Transmitter Frequency Phase (Varying Current)

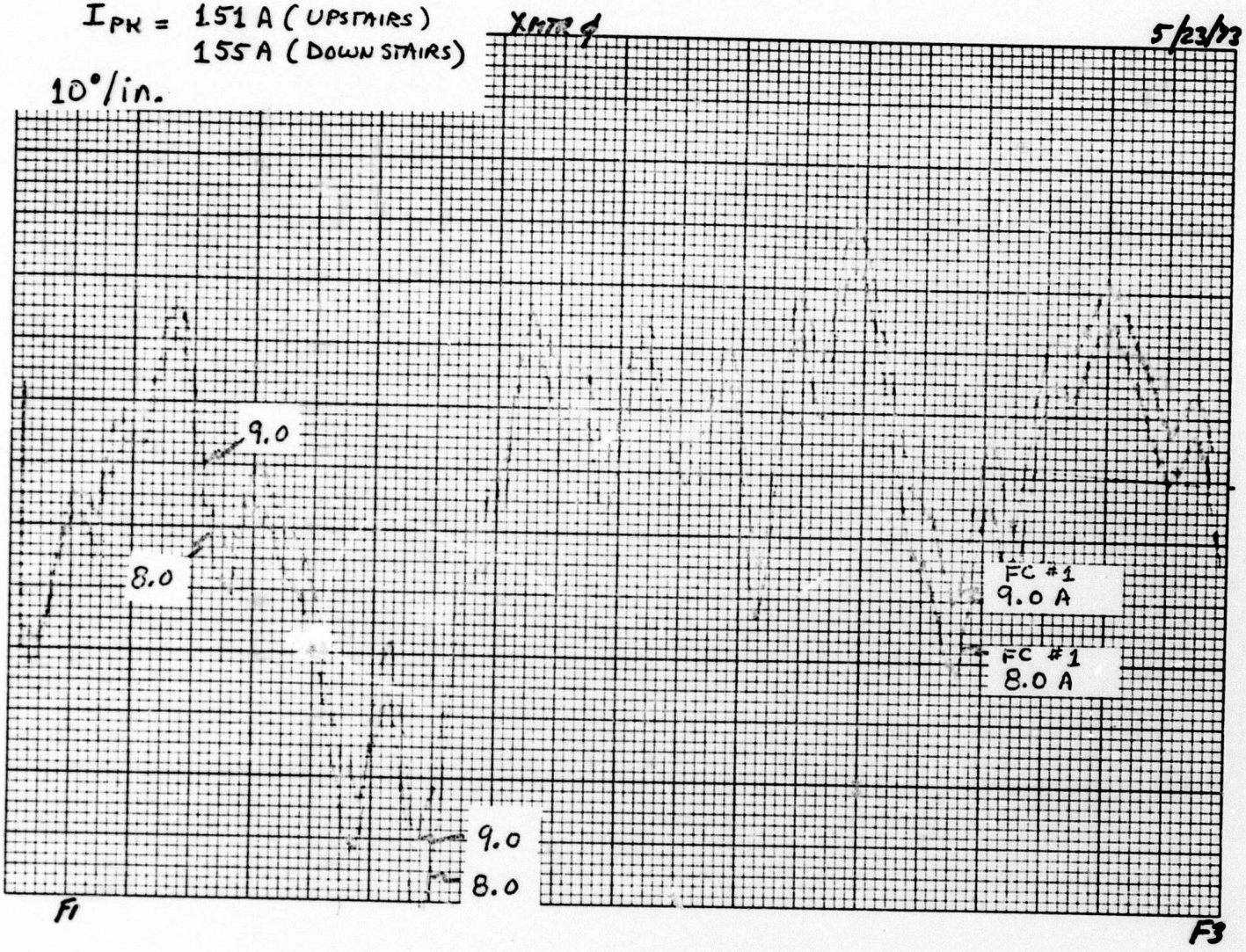


Figure 3.27 TX Frequency - Phase (Varying Focus Current)

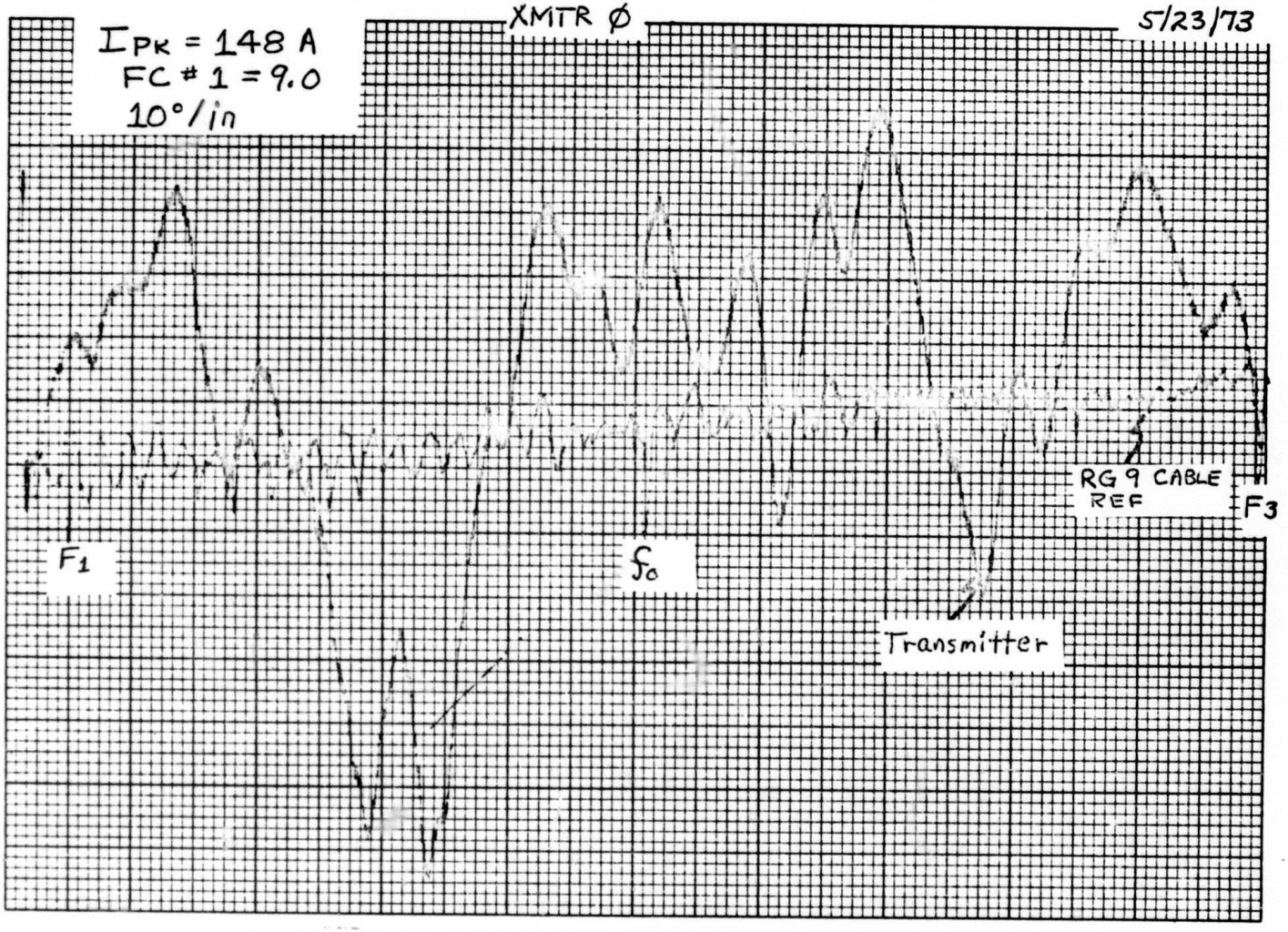


Figure 3.28 Comparison TX Phase and Coax Cable

Figure 3.26 shows the phase vs. frequency bandpass of the transmitter for different operating peak current levels of the FPA. While the fine grain phase ripple does not change significantly, the low frequency ripple peak to peak is reduced as the peak current is increased.

Figure 3.27 shows the phase vs. frequency bandpass for different Focus Coil #1 current levels. Except for a small shift in absolute phase, the two curves are essentially the same showing that phase is not critical with Focus Coil #1 current.

Figure 3.28 compares the phase vs. frequency of the transmitter against a length of RG 9 cable which is made up of a number of separate lengths connected together. While a good cable, it is far from the best possible and undoubtedly contributes a great deal to the ± 3 degrees of ripple that show in the RG 9 phase characteristics. In any event this shows the phase measurement system accuracy is probably no worse than 3 degrees.

3.3.2.2 Amplitude Versus Frequency. Figures 3.29 and 3.30 are slow frequency sweep graph data for the complete transmitter.

Figure 3.29 is a family of curves for different values of Focus Coil #1 current. Not only did power increase with increased focus coil current, but the amplitude of ripple decreased. The limit of desired level of operation is dictated by the unstable body current as noted on the graph.

Figure 3.30 compares the effect of Focus Coil #2 current on bandpass performance. Except for the difference at the lower end of the band, the two curves are identical. This result suggests that the FC #2 current should be set at 18.0 amperes instead of 19 amperes as recommended by the tube data.

Figures 3.31 and 3.32 represent data taken in slow frequency sweep on a graph recorder and then transferred to a Varian data sheet for comparison against data taken at Varian. In general the data taken at the Floyd site are lower in power level and have higher amplitude ripple although many of the peaks and valleys occur at about the same frequencies. The Varian data is taken under ideal conditions since the output load is close to the output of the tube which would account for the higher power (no circulator loss) and less amplitude ripple.

Figure 3.31 shows a progression of improvement in flatness of response. The original data is shown by Curve 2 where the drive power to the FPA was insufficient to keep the FPA in saturization. When the drive power response was improved, the FPA response likewise improved which is shown by Curve 3. Additional improvement was achieved by removing the SF6 window from the waveguide system as shown by Curve 4. The window was initially used to run the pressure on the tube side higher than the pressure on the antenna side due to limitations in the pressure capability of the feedhorn window. Subsequent investigation showed that it was possible to run the tube window at the same pressure as the remainder of the waveguide system.

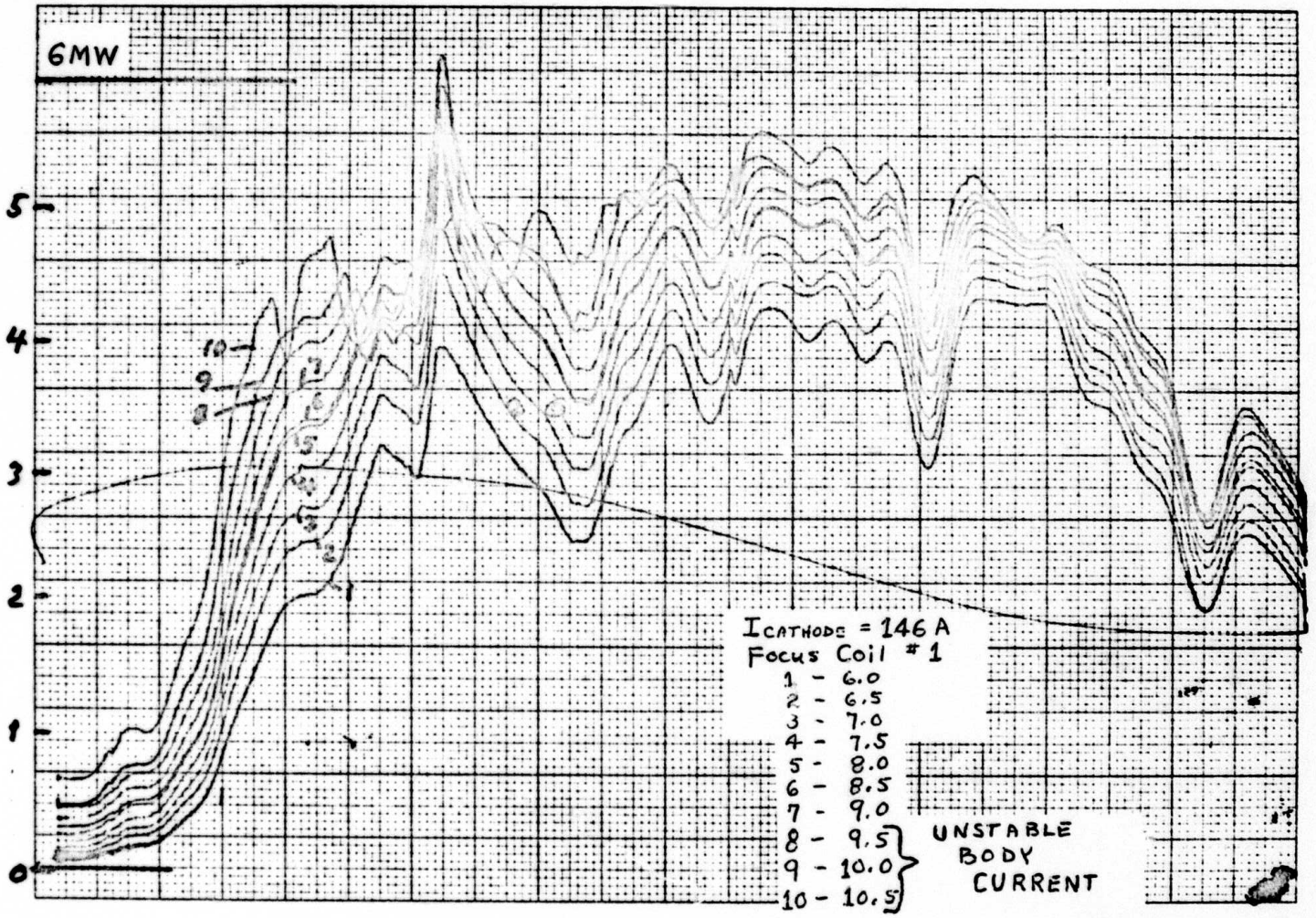


Figure 3.29 TX Frequency - Power Output (Varying Focus Current)

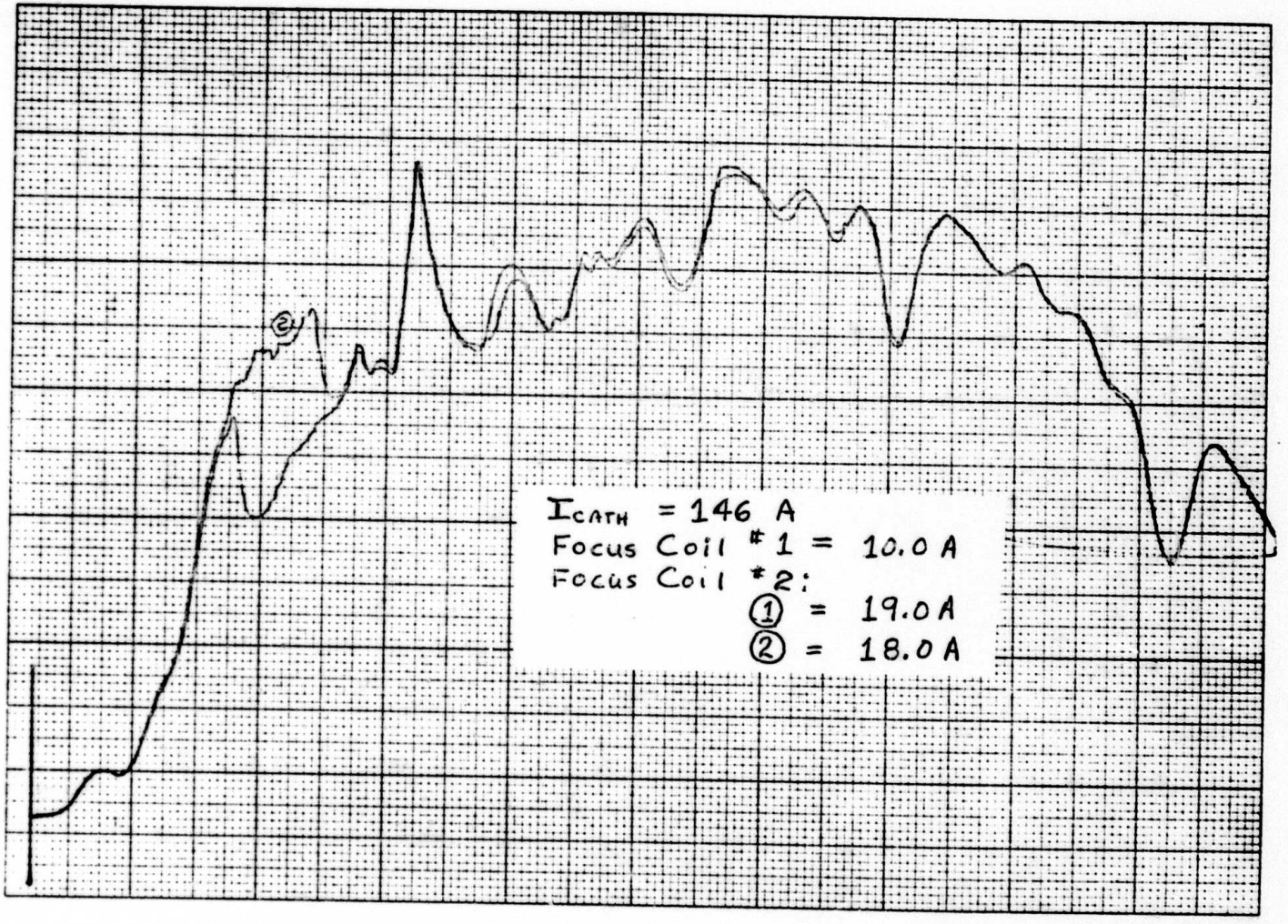


Figure 3.30 TX Frequency - Power Output (Varying Focus Current #2)

VA 914A SN 103
TUBE X-9R4
V_B 175 KV
I_B 146 A
I_{COL} 144 A
I_{COL} 2.0 A (NO RF)

VIDEO PULSE WIDTH 45 μ SEC.
R.F. PULSE WIDTH 40 μSEC
PULSE REP RATE 70 PPS.

E_F 15.0 VOLTS
I_F 37.0 AMPS
P_{DRIVE} 4000 WATTS

I_{CATH} 10.4 A
I_2 19.0 A
I_3 20.0 A
I_{COLL} 20.0 A

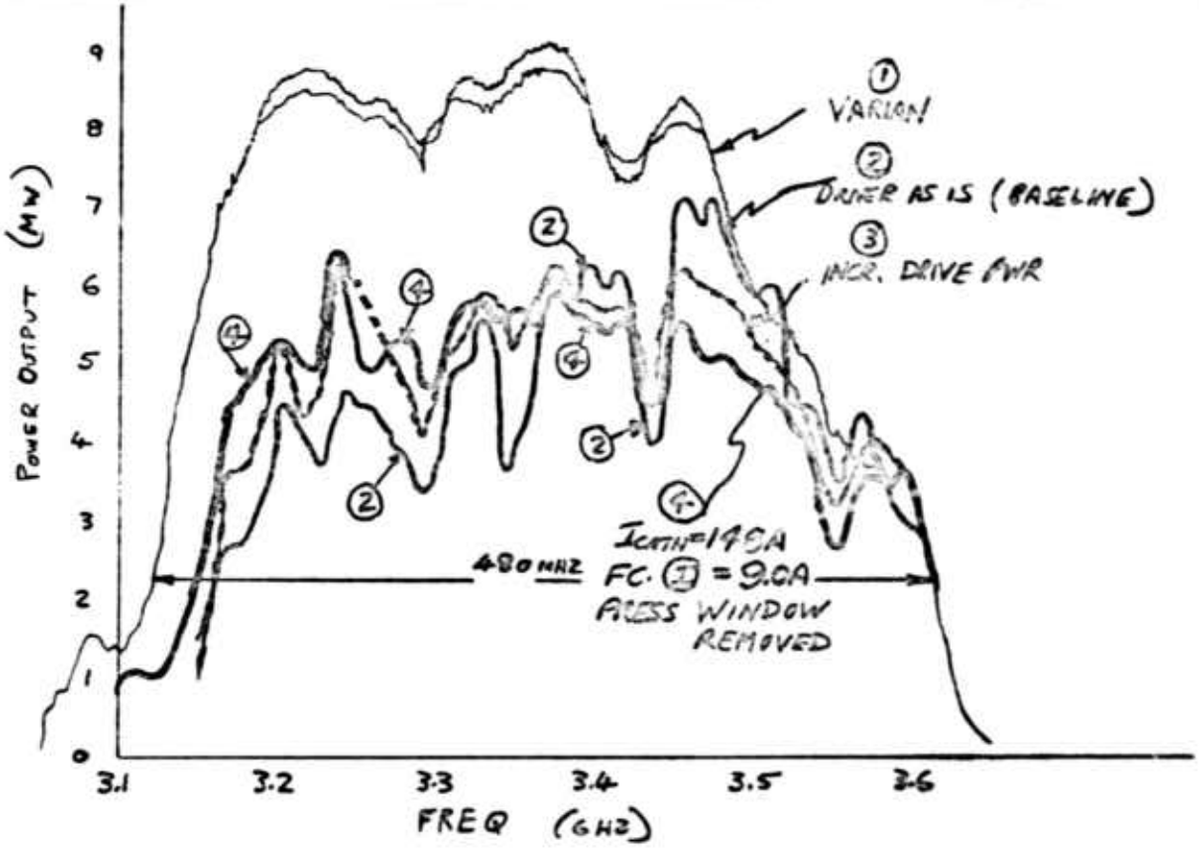


Figure 3.31 TX Frequency-Power Output (Varian Data and Floyd Performance)

YA-914A

V_B 175 kV
I_B 146 A
I_{COL} 144 A
I_{COL} 2.0 A (NO RF)

VIDEO PULSE WIDTH 45 μsec
R.F. PULSE WIDTH 40 μsec.
PULSE R[illegible] RATE 70 pps.

E_F 15.0 VOLTS
I_F 37.0 AMPS
P_{DRIVE} 4000 WATTS

I_{OTTN} 10.4 A
I_2 19.0 A
I_3 20.0 A
I_{COLL} 20.0 A

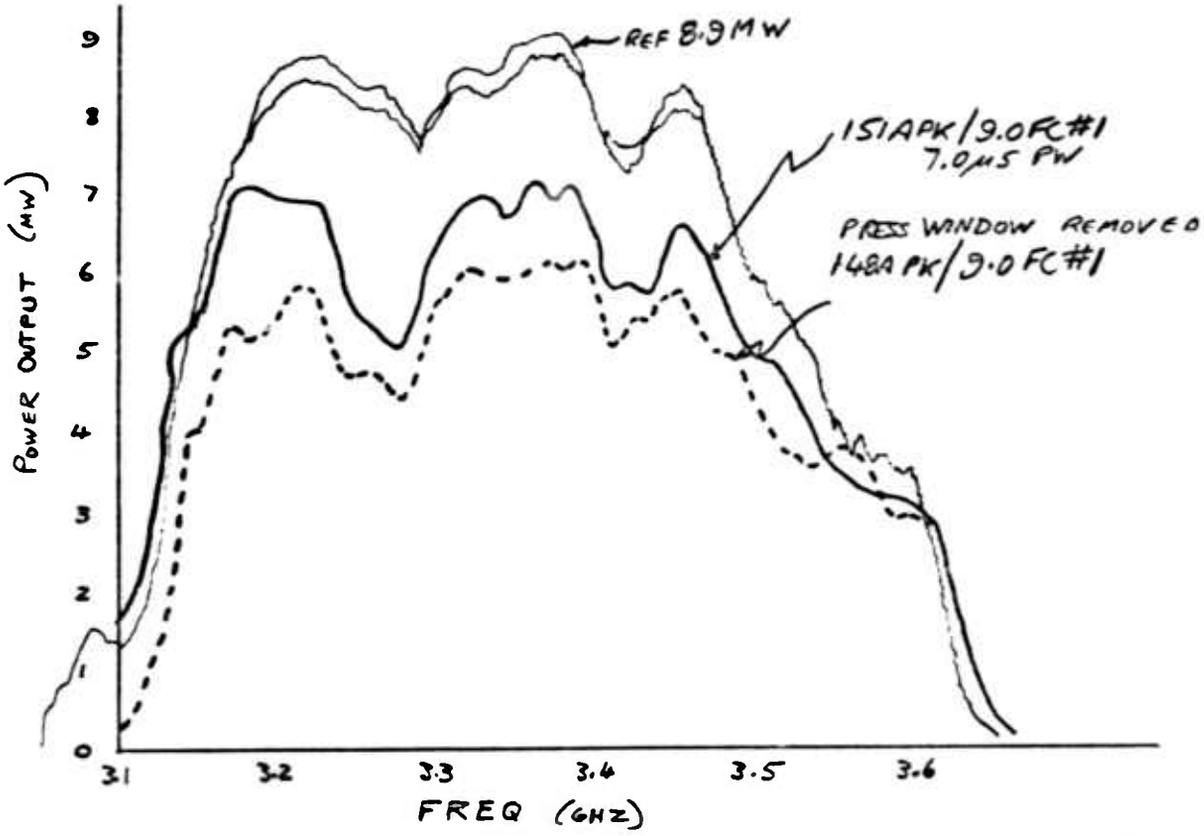


Figure 3.32 TX Frequency-Power Output (Varian Data and Optimum Floyd Performance)

Figure 3.32 shows the change in amplitude response as the peak operating current is increased. While power output increased as expected, the flatness of response did not, which is not readily explainable and inconsistent with all other data.

3.3.3 Wide Pulse Width 500 MHz Chirp Performance.

Driver Stage. Figure 3.33 shows a before/after scope photo of the Driver beam current pulse and detected rf pulse. The top photo is the result of only widening the gate to the driver modulator from the initial 20 μs to 40 μs. For the 20 μs pulse width the initial level of the pulse held up adequately but lack of drive in low level modulator circuitry resulted in a poor pulse when expanding it to the 40 μs. Changes in low level solid state circuitry resulted in the much improved performance of the bottom photo.

FPA Modulator State. Photos 1 through 4 of Figure 3.34 are of the "widened" FPA cathode current pulse showing the results of different PFN coil tapping arrangements. All arrangements use 21 capacitors. Arrangement 4 is considered adequate for the requirement.

Vertical Scale: 50 amperes/division

Horizontal Scale: 10 microseconds/division

Photo 1 Arrangement:
(Figure 3.34)

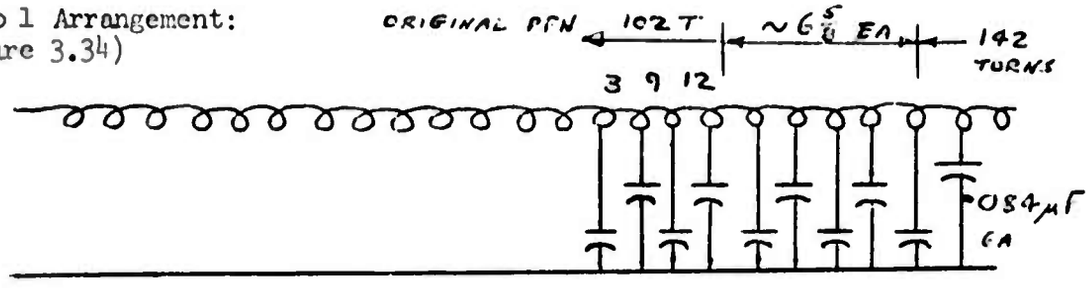
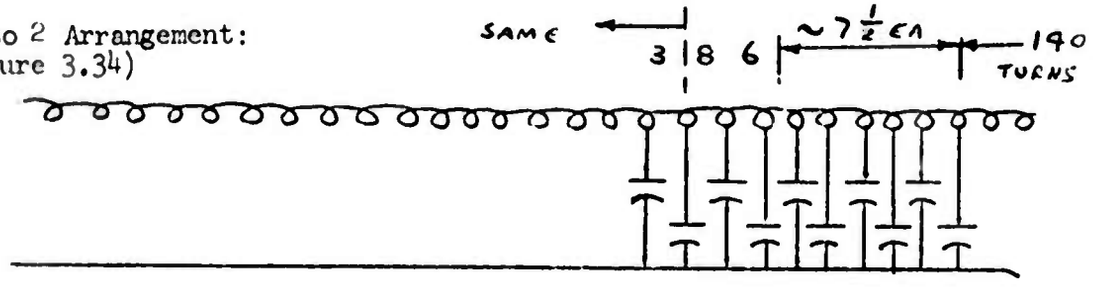
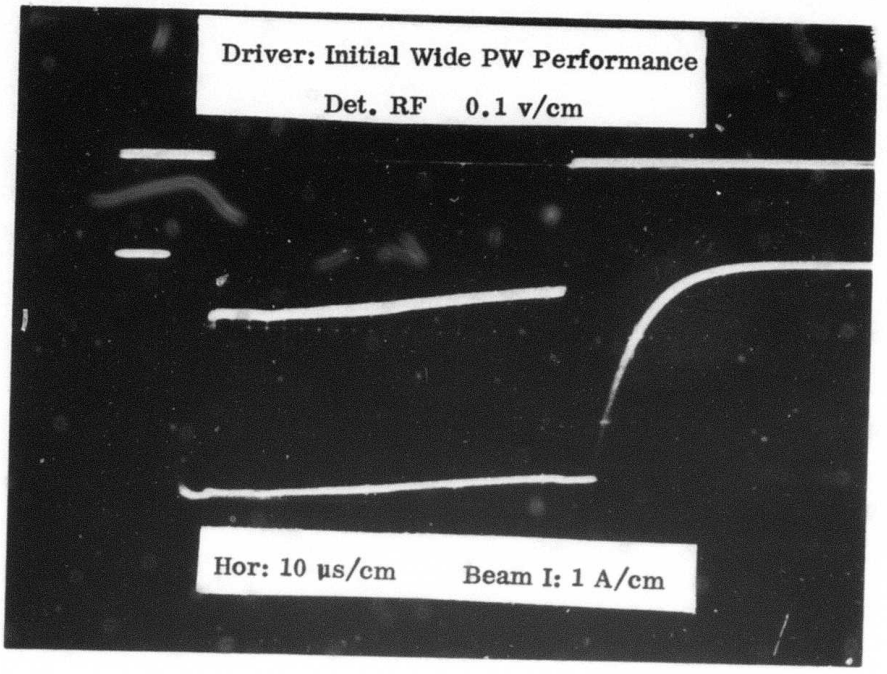


Photo 2 Arrangement:
(Figure 3.34)





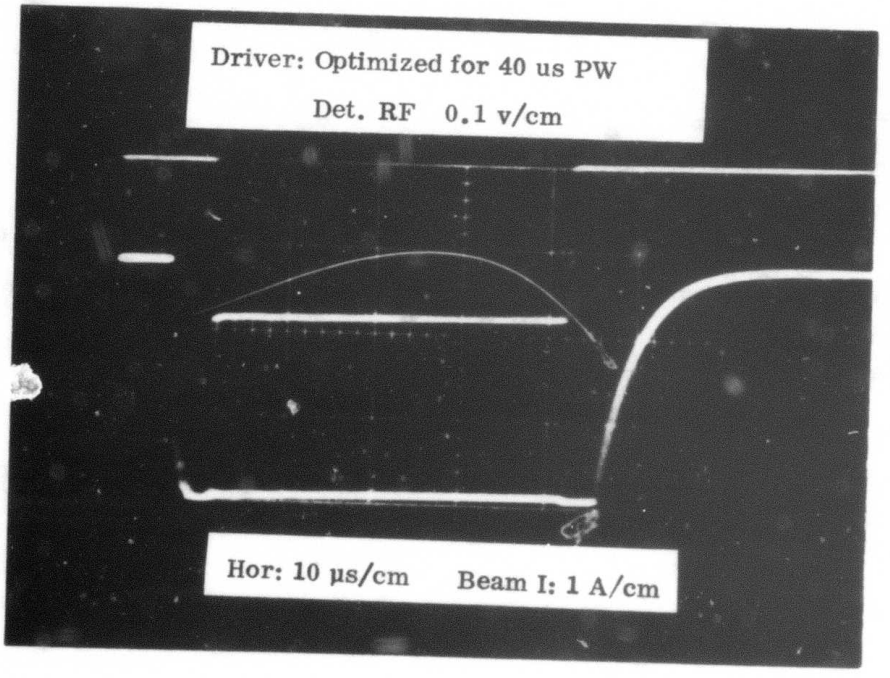


Figure 3.33 Driver Waveforms 20 and 40 µsec

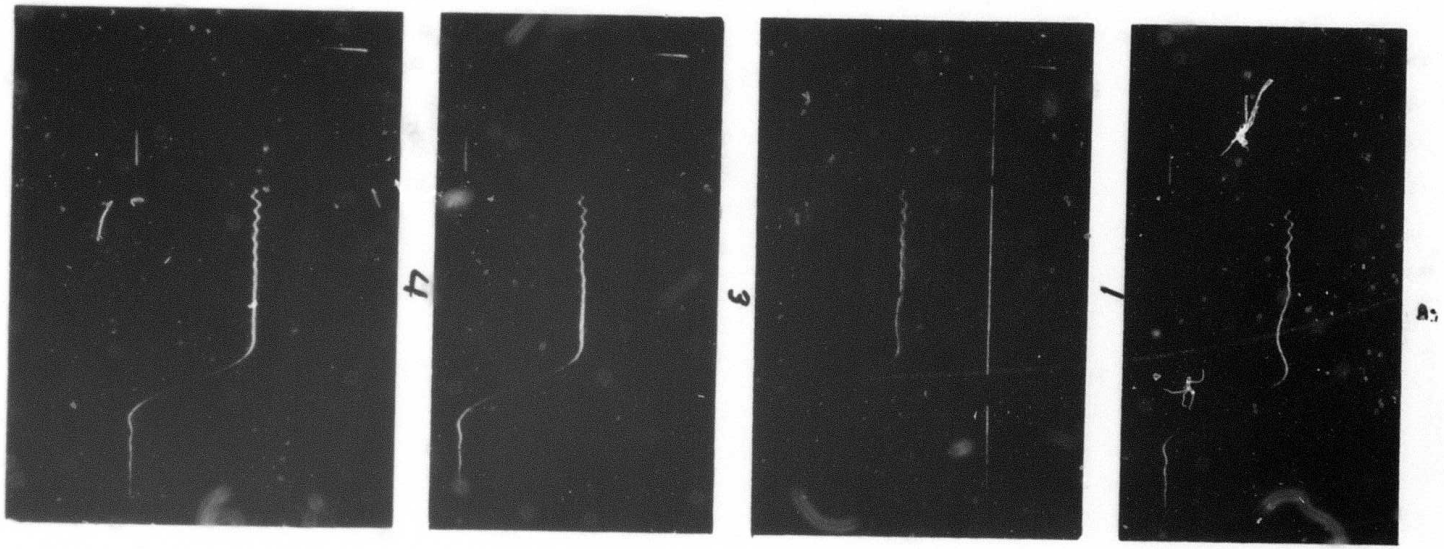


Figure 3.34 FPA Cathode Current for 40 μsec Pulse and Varying Line Lengths

Photo 3 Arrangement:
(Figure 3.34)

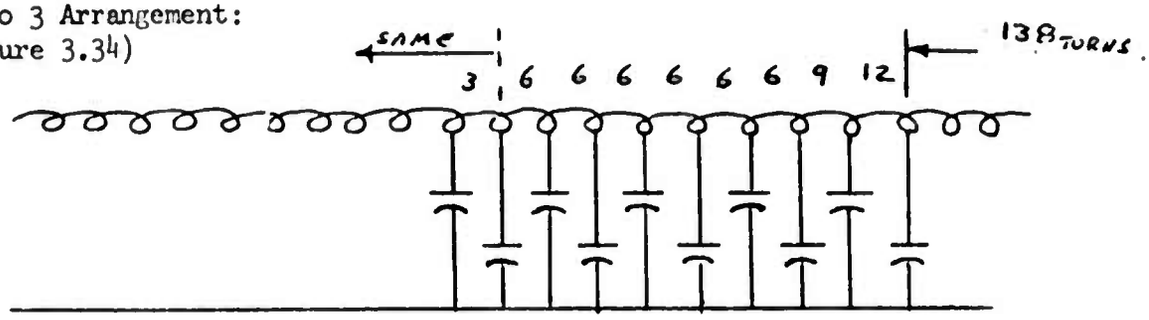
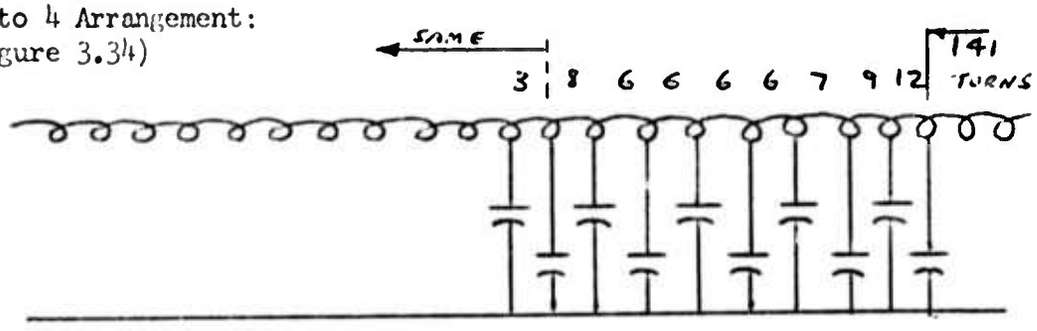


Photo 4 Arrangement:
(Figure 3.34)



Transmitter Chirp Performance. Photos 5 through 8 of Figure 3.35 depict the rf chirp performance of the transmitter. It should be noted that frequency sweep is high to low frequency which is opposite from the slow frequency tests.

Photo 5 is the detected rf FPA output pulse before equipment improvements; i.e., 250 MHz chirp 20 usec pulse. Horizontal scale is 5 us/division.

Photos 6 through 8 are of the detected RF FPA Output pulse after equipment improvement and the pulse width widened and the frequency band increased to nominally 500 MHz chirp, 40 usec pulse width.

Operating parameters for these photos are:

I_{PK}:	147 amps
I_{BAV}:	.496 amp
I_{BODY}:	8.5 ma
P_{AV}:	12.5 kw (meter)
E_B:	16 kv
I_{DC}:	5.0 amps

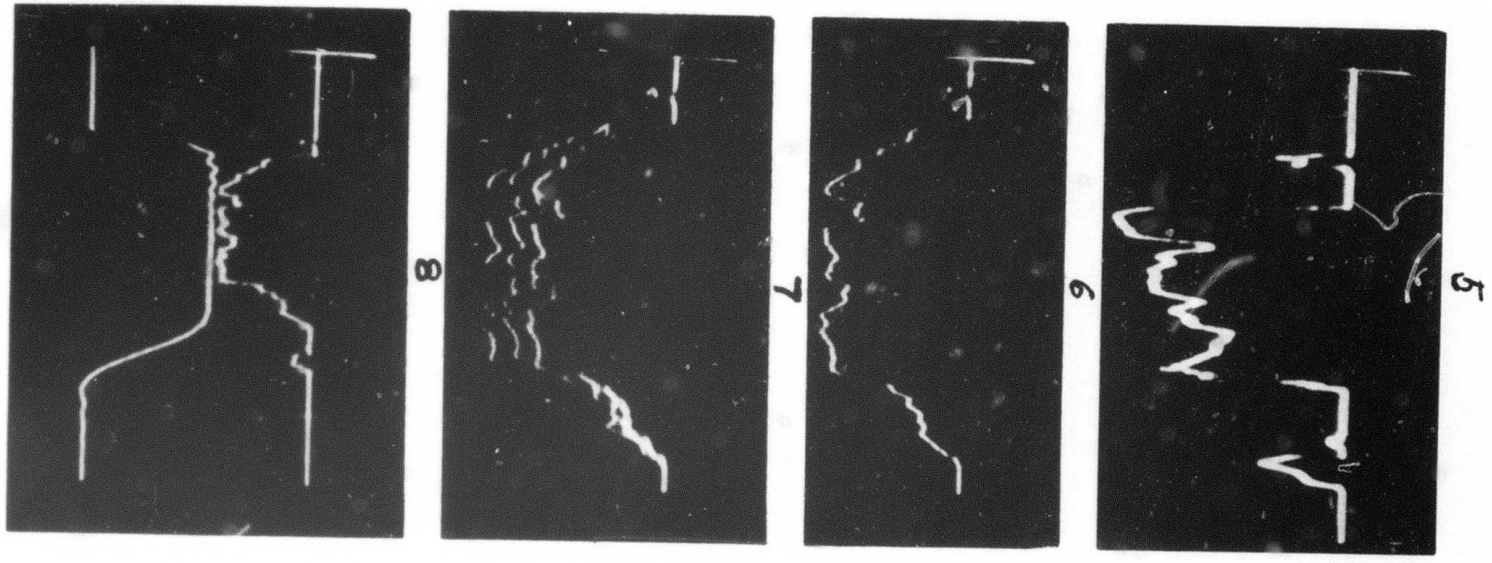


Figure 3.35 40 μsec Transmitter Chirp Performance

Horiz. Scale:	5 us/div (6 & 7)
Vert RF Det. Scale:	.2 V/div
Vert Peak Amp Scale:	50 A/div
f_1:	3350 MHz
f_o:	3350 MHz
f_h:	3590 MHz

Photo 6 is the detected rf output for the above operating conditions. Improvements in flatness can be noted over Photo 5. Improvement in amplitude can also be seen by comparing main pulse to amplitude of "rabbit ears" which are of equal power for both photos 5 and 6. A comparison made with slow sweep amplitude curves shows a close correlation to these chirp photos.

Photo 7 is the same as 6 except showing 1 db steps in amplitude which provides a means of measuring pulse flatness.

Photo 8 shows the relative timing of the cathode current and detected rf pulse. It can be seen from this photo that there appears to be little gained in widening the video pulse. The rf pulse shape is primarily controlled by the rf bandpass of the FPA tube.

3.4 Synchronizer

3.4.1 Introduction. System timing and radar control functions are generated in two digital logic assemblies. One comprises medium-speed logic and provides mode control and the bulk of the radar timing. This unit, referred to as the "synchronizer", is a rebuilt and redesigned version of the original and operates essentially the same as its predecessor. The second unit, designated "HISYNC" (for high-speed synchronizer), derives the transmit and receive 10 MHz digital clocks, and generates certain precisely-tuned, low-jitter signals required in the FM mode of operation. The HISYNC was newly procured for the upgrade program and is described in detail in Section 4.4.

3.4.2 General Description

The synchronizer chassis is the prime source of system timing and mode control for the radar, and comprises twelve plug-in module boards, each of which accepts up to sixty DIP integrated-circuit logic packages. At the onset of the upgrade program, the overall synchronizer underwent several improvements in the areas of wiring layout, power supply filtering and general workmanship. Specifically, each plug-in board received a treatment of gold plate along the connector etch to improve the contact of the existing copper surface which was deteriorating. Additional filter capacitors

were placed around the periphery of the power bus etch to reduce noise and signal coupling, and the ground etch was augmented by soldered bus wires in parallel to form a grid configuration. In the final design, all unused input pins to the logic elements were tied to a logic "1" voltage as dictated by normal practice. On the synchronizer chassis all module connectors were replaced by new ones, and the existing harness wiring was stripped out and rewired. Additional grounding points were provided on the chassis which were wired through the connectors to mating pins on the ground busses on the module boards.

The synchronizer operates on two 10-MHz clocks generated in the HISYNC logic. One is fixed with respect to the system sync pulse, and drives the transmit-time counter. The other varies in phase in 6.25 ns steps with respect to the reference clock, and drives the range-timing counter. The original version of the synchronizer utilized only the reference clock, consequently there was a range skew of 0.1 us maximum in the displayed target return. Inasmuch as the two clocks are basically asynchronous, it was necessary to provide additional logic to insure proper timing of the starting of the range-time counter with respect to the range-delay counter which is also driven by the reference clock. This was accomplished through the use of switched delay lines of 25, 50, and 75 ns delays which are controlled by the respective range word bits supplied from the range tracker. The start pulse generated by the reference clock is thus made to track within 25 ns the phase of the variable clock. The setup time of the logic flip-flops accommodates a variation of 25 ns.

The basic operating modes of the new system are the same as the original except that a look-ahead display mode has been added which enables an operator to view a target in the next higher FM bandwidth while it is being tracked in a lower bandwidth. The bandwidths of 5, 50 and 500 MHz are each provided with eight steps of manually-selectable range offsets so that the operator may insure a target being in the center of the range window before initiating range-tracking in the next higher bandwidth. The logic required for the look-ahead display mode comprises basically a 25-bit full adder inserted between the range word register in the range tracker and the range-delay counter in the synchronizer. When the display mode is selected, the look-ahead duty cycle is one out of eight PRI's.

In the original design of the synchronizer logic it was necessary to wire all fourteen bits of the 10 MHz range-timing counter to each "aud" gate from which a time interval was to be generated. In order to minimize the effort required for future timing changes the direct binary form of decoding was replaced by two-level decoding wherein only four wires were ultimately required to decode a specific time delay. The first level of decoding was accomplished in three groups of four sequential flip-flops each, beginning with the least significant bit (LSB) of the counter, and one group of two flip-flops which were the most significant bits (MSB's) of the counter. From each group of four flip-flops, sixteen different time delays were decoded, and from the group of two flip-flops four different time delays were decoded. Thereafter, any time delay within the total range of the counter could be subsequently decoded by selecting only four specific time delays, one from each of the four groups. Thus, four-input "and" gates could be

utilized for all timing and signal generation.

3.5 Range Error Processor - Figure 3.36

The range error processor (REP) derives range-error information from detected target video through the familiar early gate-late gate method wherein signal energy in one-half the range window is integrated and stored, and subtracted from integrated signal energy in the other half. Thus, a point-source target centered in the range window ideally yields a zero-voltage output which is recognized as a zero error in the tracking loop.

The REP underwent several component substitutions but the overall circuit configuration remained much the same. The FET switches of mid-1960 vintage were replaced with COSMOS versions possessing significantly lower leakage currents. The integrating operational amplifiers were replaced with high-impedance FET models intended specifically for integrate-and-hold applications. The driver circuits for the FET switches were redesigned to maintain compatability with the early and late gates generated in the high-speed synchronizer.

The output signals of the REP originally were two voltage levels representing respectively the summed energy in the entire range window, and the difference of the energies in the two halves of the range window. These two outputs were then fed to an analog divider which yielded a normalized error voltage by the process of dividing the sum voltage into the difference voltage. For fixed range offsets, this derived error voltage was relatively insensitive to amplitude variation of a point-source target, but was affected by target energy-spreading arising from multiple returns within the range window. The effect was to lower the error-gain of the REP thus making the range tracker appear to react somewhat sluggishly.

The approach taken in the re-design of the REP was to employ an interim method of utilizing only the difference voltage as the final error signal. The anticipated advantage and disadvantage of this scheme was opposite to that of the normalization method in that amplitude variations would be the critical factor. It was felt however, that the improved receiver AGC system would minimize target amplitude variations and thus provide some compensation. The requirement for additional smoothing was anticipated because of the fact that the early and late gates could be positioned around the target in 6.25 ns time increments instead of the previous 0.1 μs steps.

The extent of testing possible on the REP was to manually slew a test pulse through the range window while the range tracker was verified to have maintained lock-on. A final test was to verify that the range tracker could maintain lock-on of a stationary target for approximately three days.

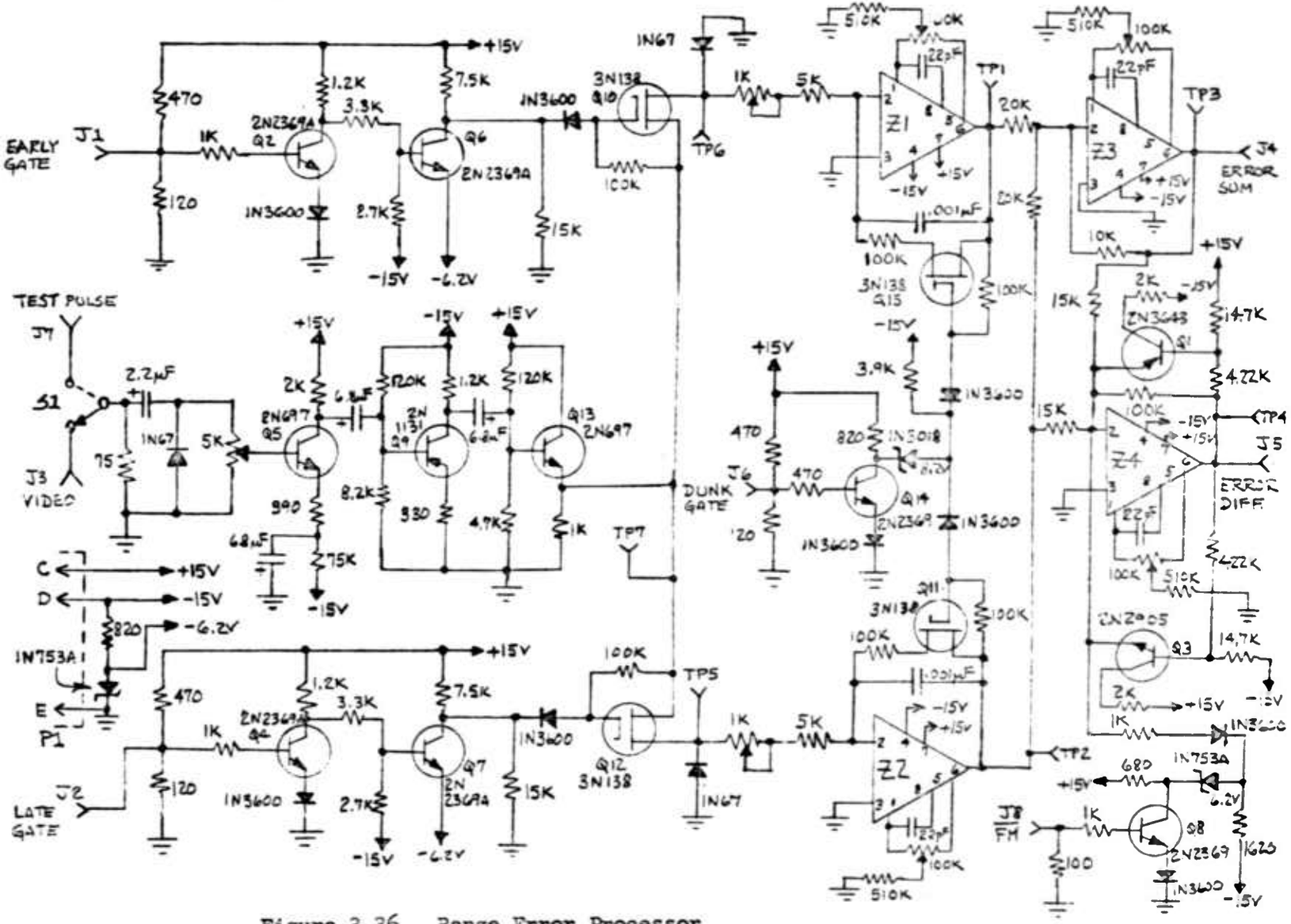


Figure 3.36 Range Error Processor

3.6 Software

The satellite tracking of targets of interest is currently performed using a data tape on the PDP-1 site computer that is prepared using the Honeywell GE 645 computer at Building 3, RADC.

The input elements for the satellite ephemerides are received from ENT AFB over the teletype network and punched out on 5 cards for each satellite. For many years these were transmitted when the data was in 10 secs. time error along the orbit for the particular satellite. Recently this was changed to 1 sec which resulted in very frequent updates and a consequent heavy Comms and TTY load throughout the network.

To resolve this problem ADC reduced the number of cards to 2 by deleting some data that was not essential to most users and deleting other data that could be calculated at the sites. Using a program that was originally written in Fortran IV for use at RCA Moorestown the Program shown in Figure 3.37 a and b was developed. Several modifications were required to produce the data required for use in the test facility programs. The program and data results are shown in Figure 3.38 a, b and c. During the cutover phase from 5 to 2 cards both sets of data were sent. The comparative data is shown, 2 card as received, 5 card as calculated and 5 card as received. Small differences in the 5 card calculated data result from a different decimal point in the exponent quantities and the omission of unwanted data from the reconstituted 5 card set such as cross section and estimated life which have been omitted from the 2 card set and cannot be reconstructed.

The data output is only presented in printout format since the primary goal was to verify that the conversion routines could be made. To use the data a punched card, or tape output would be required.

3.7 Short Pulse Tester

For the most part, the various components used in the Wideband portions of the radar at the test facility were tested for amplitude and phase ripple by using a Hewlett-Packard Network Analyzer. This extremely useful and versatile device was employed also to measure VSWR of the various wide-band components. However, it does require that any device being measured has the same input and output frequency.

Thus measuring the wide-band performance of devices such as mixers and converters poses a special problem. Likewise, components whose output terminal is difficult to reach, such as an antenna, present a difficulty in test analysis.

Hence, a short-pulse tester was developed and built at the test facility to assist in evaluating several components of the type mentioned above. Briefly, generation of the Short Pulse Tester can be explained by referring to the Block Diagram in Figure 3.39.

```
      C     SUBROUTINE C0N52
            REAL*8 DXN,DEC,SM,RD,E2AB,E2SD,E2A0
            INTEGER*4 ELSET(8),E2END(7)
            DATA E2END/'E ','N ','D ','C ','A ','R ','D '/
     66     F0RMAT(15X,4(E15.8,5X))
     6666 F0RMAT (8A1,1X,A2,A3,A3,1X,I2,I3,F9.8,1X,F10.8,1X,E8.5,12X,I4)
     6667 F0RMAT(2X,I5,1X,D8.4,1X,F8.4,1X,D7.7,1X,2(F8.4,1X),D11.8,I5)
     6668 F0RMAT ( H0, 8A1,1X,A2,A3,A3,1X,A2,I3,F9.8,1X,F10.8,1X,E.5,2X,I5)
     6669 F0RMAT (2H 2,1X,I5,1X,2(F8.4,1X),F7.0,1X,2(F8.4,1X),F11.8,I5)
     7000 F0RMAT (2H01, 1X,I5,4X,I5,1X,A3,2X,A3,1X,I5,13X,I6)
     7001 F0RMAT (2H 2,1X, I5, 1X,I5,F9.8,1X,3(F8.4,1X),1X,F8.7,1X,F8.4)
     7002 F0RMAT(2H 3,1X,I5,1X,F11.8,1X,F11.9,   2(F9.5),1X,5PE .0)
     7003 F0RMAT(2H 4,1X,I5,25X,3(5PE .0))
     7004 F0RMAT(2H 5,1X,I5,1X,F11.8,1X,2(7PE .0,1X))
     7005 F0RMAT (1X,69A1)
     7006 F0RMAT (1X,I1,69A1)
     7007 F0RMAT (1H0 )
            DIMENSI0N CARDSET (69)
      C     C0MPUTE FRACTI0NS
            E2TQ= 4./3.
            E2TQM= -4./3.
            E2TH= 3./2.
            E2THM=-3./2.
            E20T= 1./3.
            E20TM=-1./3.
            E2K=.0743667785
            E2J2=1082.549E-6
            E2A =1.
            E2V =.004363323
            PI=3.141592654
            TPI=2.*3.14159265
         16 C0NTINUE
            READ6666 ,(ELSET(I),I=1,8),IDA,IDB,IDC,YD,JD,FD,RDR,XMMA,NE
            D0 10 I=1,7
            IF(ELSET(I).NE.E2END(I)) G0 T0 15
         10 C0NTINUE
            G0 T0 200
         15 READ6667 ,NS,DXN,RA,DEC,AP,AN,RD,NR
            XN=DXN
            EC=DEC
            RRID=DXN*.0174532925
            RRI=XN*.0174532925
            S2RRI=(SIN(RRI))**2
            S2RRID=(SIN(RRID))**2
            DE=RD*E2V
      C     C0MPUTE SEMI-MAJ0R AXIS
            E2A0=(E2K**2/DE**2)**E20T
            E2SD=E2THM    * F2J2*(1.     /E2A0**2)*(1.-DEC**2)**E2THM*
           1(1.-(E2TH)*S2RRID)
            E2AB=E2A0*(1.+(E20T )*E2SD-(E20T )*E2SD**2)
            SM=E2AB
      C     C0MPUTE FIRST DERIVATIVE 0F THE RIGHT ASCENSI0N
            E2TMP= E2TH*E2J2*( (E2A/(E2AB*(1.-EC**2)))**2)*RD
            E20M=-E2TMP*C0S (RRI)*360.
            RAR=E20M
      C     C0MPUTE FIRST DERIVATIVE 0F THE ARGUMENT 0F PERIGEE
            E2WD=E2TMP*(2.-2.5*S2RRI)*360.
            APR=E2WD
      C     C0MPUTE EARTH RADII/DAY
            E2AD= E2TQM    *(E2AB/RD)*RDR
```

Figure 3.37a Fortran Listing 2 Card to 5 Card Conversion (Sheet 1 of 2)

```
      XISR=E2A0
C     COMPUTE EARTH RADII/DAY**2
      PART1=2.*E2AB/RD
      PART2=10./(9.*R0)
      PART3=PART2*RDR**2
      PART4=XMMA*PI
      E2ADD=PART1*(PART3*PART4)
      XISA=2*E2ADD/PI
C     COMPUTE FIRST DERIVATIVE OF THE ECCENTRICITY
      E2ED= (E2TQM )*((1.-EC)/RD)*RDR
      XIER=E2E0
C     COMPUTE  SECOND DERIVATIVE OF RIGHT ASCENSION
      PART5 = (1.+E2TQ * (1.-EC)     /(1.+EC)) *RDR
      OHMDDO = (RAR/RD)* PART5
C     COMPUTE  SECOND DERIVITIVE OF ARGUMENT OF PERIGEE
      WDDO = (APR/RD) * PART5
C     COMPUTE  SECOND DERIVITIVE  OF ECCENTRICITY
      PART6=2./(9.*RD)
      PART7=PART6*(RDR**2)
      PART8= PART7*XMMA
      PART9 =    4. *(1.-EC)/RD
      EEDDO = PART9 * PART8
C     CONVERT  EPOCH YR AND DAY TO NDAE.ALSO TRUE JULIAN DAY CORRECTION.
      NDAE    =((YD-70)*1000) + JD
      TJD=42047. + JD
      PRINT7007
      PRINT6668 ,(ELSET(I),I=1,8),IDA,IDB,IDC,YD,JD,FD,RDR,XMMA,NE
      PRINT6669 ,NS,DXN,RA,DEC,AP,AN,RD,NR
      PRINT7000 ,NS,NE,IDB,IDC,NR,NDAE
      PRINT7001 ,NS,TJD,FD,AN,RA,AP,EC,XN
      PRINT7002 ,NS,RD,RDR,RAR,APR,XIER
      PRINT7003 ,NS,OHMDDO,WDDO,EEDDO
      PRINT7004 ,NS,SM,XISR,XISA
      PRINT7007
      DO 55 C=1,5
      READ7005 ,CARDSET
      PRINT7006 ,C,CARDSET
   55 CONTINUE
      GO TO 16
  200 NE=9999
      END
```

Figure 3.37b Fortran Listing 2 Card to 5 Card Conversion
(Sheet 2 of 2)

```
LOADING WAS COMPLETED
 R0V                                                    ← OBJECT #

1 06660U 73 34   8 8  18.88324642  .00000601 .66919E-07       94
2  6660  81.2298 199.1763       0.  250.0215 109.5879 14.02699942 3287   } 2 CARD SET

1  6660       94  34    8  3287                  4018
2  6660 42065.88324642 109.5879 199.1763 250.0215  .0046622  81.2298
3  6660 14.02699942  .000006010  -.96394 -2.79361 -56862.E-11
4  6660                         -95858.E-11 -27781.E-10 -18994.E-12
5  6660  1.13888999 -6506240.E-13  -2173301.E-14                  } 5 CARD RECONSTITUTED SET REPUNCH

1 06660 U 00094 73   34   8 0       06.9 003287 4018        0        0 7
2 06660 42065.88324678 109.5879 199.1763 250.0215 .0046622 081.2298 3
3 06660 14.02699942  .000006013 -0.96393 -2.79360 -56895.6            0 7
4 06660  66919685.7              0 -95914.6 -27797.5 -18993.7          4
5 06660 01.13889071 -6510118.6 -2173264.7 5                            } 5 CARD SET FROM ENT REPUNCHED TO REMOVE "2"


1 01085U 65   /  A 8  17.59191704  .00004946 -.49076E-06      647
2  1085  31.7530 130.6656       0.  45.0670 315.6035 15.2476951848957

1  1085       647   9    A 48957                  4017
2  1085 42064.59191704 315.6035 130.6656  45.0670  .0075285  31.7530
3  1085 15.24769518  .000049460 -6.53794 10.05405 -42925.E-10
4  1085                         -49062.E-09 75447.E-09 12778.E-11
5  1085  1.07476093 -4657017.E-12  1396417.E-13

1 01085 U 00647 65    9   A 0       06.2 048958 4017        0        0 6
2 01085 42064.59191714 315.6036 130.6656 045.0670 .0075285 031.7530 8
3 01085 15.[illegible]9518  .000049468 &6.53791 10.05401 &4293285          0 6
4 01085 &4907690456              0 &4907084  7546054  1277856              0
5 01085 01.07476140 &465783385  138678856 2                                 } 5 CARD SET FROM ENT. "2" IS = "-"


1 01620U 65 81  A 8  13.74098349  .00002624 .25988E-06      673
2  1620  87.3582 120.0222       0.  53.0624 312.0918 14.2550137242197

1  1620       673  81    A 42197                  4013
2  1620 42060.74098349 312.0918 120.0222  53.0624  .0565145  87.3582
3  1620 14.25501372  .000026240  -.30449 -3.26795 -23156.E-10
4  1620                         -12279.E-10 -13178.E-09 -68799.E-12
5  1620  1.12673412 -2765390.E-12  -8215949.E-14

1 01620 U 00673 65   81   A 0       07.2 042197 4013        0        0 6
2 01620 42060.74098352 312.0918 120.0222 053.0624 .0565145 087.3582 3
3 01620 14.25501371  .000026247 &0.30447 &3.26796 &2316285          0 6
4 01620  2598888056              0 &1228165 &1318154 &6880167          1
5 01620 01.12673448 &276614585 &821507957 9


1 01620U 65 81  A 8  20.05816983  .00003316 .27191E-06      674
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1  1620       674  81    A 42287                  4020
2  1620 42067.05816983 330.9741 118.0942  32.4877  .0564811  87.3534
3  1620 14.25540184  .000033160  -.30506 -3.26801 -29263.E-10
4  1620                         -15546.E-10 -16654.E-09 -71983.E-12
5  1620  1.12671314 -3494516.E-12  -8595583.E-14

1 01620 U 00674 65   81   A 0       06.8 042287 4020        0        0 0
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3 01620 14.25540184  .000033166 &0.30505 &3.26800 &2926985          0 4
4 01620  2719166756              0 &1554855 &1665754 &7198487          8
5 01620 01.12671403 &349519385 &859395567 3
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Figure 3.38a Comparison of Supplied and Regenerated 5 Card Data
(Sheet 1 of 2)

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1 02253U 66 56 A  B  19.14277124  .00009055 .88490E-07      132
2  2253  85.8587 312.3984       0. 167.9545 193.8937  7.99622974022098

1  2253       132  56    A  22098                    4019    *
2  2253 42066.14277124 193.8937 312.3984 167.9545  .0699192  85.8587
3  2253  7.99622974  .000090550  -.12425  -.83783 -14043.E-09
4  2253                          -30379.E-10 -20485.E-09 -41065.E-12
5  2253  1.65637956 -2500931.E-11  -7302049.E-14

1 02253 U 00132 66   56  A  0       03.3 022098 4019        0       0 3



2 02253 42066.14277149 193.8937 312.3984 167.9545 .0699192 085.8587 1
3 02253 07.99622973  .000090558 50.12424 50.83783 51404484          0 9
4 02253  8849013787            0 53038085 52048584 54106487          5
5 02253 01.65638008 525011608+ 5723770087 0


1 02253U 66 56 A  B  21.26970291  .00000035 .60095E-07      134
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1  2253       134  56    A  22115                    4021
2  2253 42068.26970291 197.2812 312.1394 164.9915  .0699718  85.8468
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4 02253  6009504087            0 51183987 57959687 52795987          5
5 02253 01.6[illegible]3254 5972108087 5497975087 9


1 06660U 73 34  B B  18.88324642  .00000601 .66919E-07      94
2  6660  81.2298 199.1763       0. 250.0215 109.5879 14.02699942 3287

1  6660        94  34    B  3287                    4018
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3  6660 14.02699942  .000006010  -.96394 -2.79361 -56862.E-11
4  6660                          -95858.E-11 -27781.E-10 -18994.E-12
5  6660  1.13888999 -6506240.E-13  -2173301.E-14

1 06660 U 00094 73   34   B 0       06.9 003287 4018        0       0 7
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3 06660 14.02699942  .000006013 50.96393 52.79361 55689586          0 8
4 06660  6691968587            0 59591486 52779785 51899387          4
5 06660 01.13889071 5651011886 5217326487 5

FORTRAN RUN-TIME ERROR IN '98COREAD' CALLED AT LOC X'02ABA'.
END-OF-FILE ON UNIT 105

 FIN
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Figure 3.38b Comparison of Supplied and Regenerated 5 Card Data
(Sheet 2 of 2)

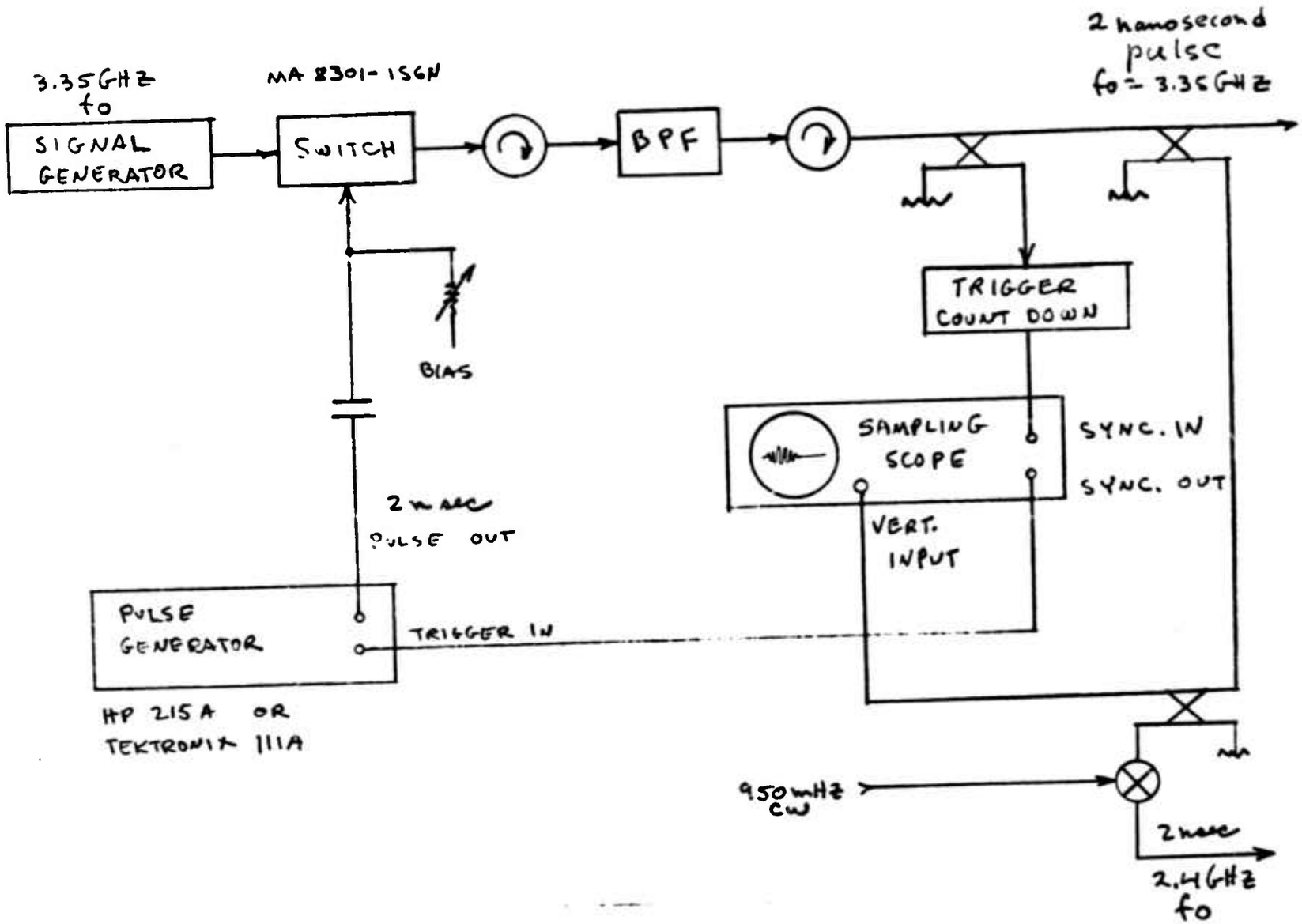


Figure 3.39 Short Pulse Tester, Block Diagram

A cw signal source such as an HP 608D is set to either 2.4 GHz or 3.35 GHz center frequency depending on where the short pulse tester will be used. The output level is adjusted to minimize the insertion loss thru the Watkins-Johnson MIJ or MIK mixer, usually +10 dbm or higher.

The modulation waveform, a two nanosecond pulse from the HP 8003A pulse generator, is adjusted in amplitude and shape (rise and fall times) to produce an RF output waveform having very low (-40db) sidelobes. Figure 3.40 shows the actual waveform developed by the short pulse tester built and used at the test facility radar. The fine-grained structure appearing in the baseline of Figure 3.40 is the CW leakage thru the mixer, and is minimized by adjusting the bias and observing the oscilloscope. Signal-to-noise ratios greater than 45 db have been achieved with the configuration shown.

Two methods are available for utilizing the short pulse tester output for reflection or transmission measurements. One is to connect the unterminated front of the output circulator to the oscilloscope. In this manner, the transmit pulse is observed by means of the leakage thru the isolator (about 26 db) while the reflected pulse is observed at some time later, depending on the electrical distance from the mismatch.

Thus, the tester acts as an RF time domain reflectometer and can be gainfully used to disclose defects, mismatches and the like, present in waveguide runs, long cable runs, antenna feed horns, etc.

The incident and reflected pulses may be presented alternately on the sampling scope by extracting a portion of the signal by means of directional couplers as shown in the block diagram.

In the case of analyzing the transmission characteristic of a mixer where the input and output frequencies are dissimilar, phase measurements are quite difficult and cumbersome to analyze since the two frequencies seldom have an integral relationship to each other.

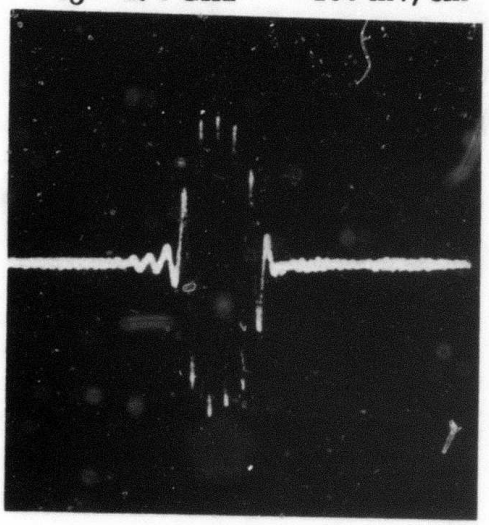
In a case like this, the weighted short pulse is impinged on the input to the mixer, the mixer is operated in its normal fashion, and observations are made of the output signal.

Although quantitative results are not usually obtained, this device is useful in studying any degradation occurring in the mixer under conditions which simulate actual use.

Figure 3.40 shows the dispersive effect of ten feet of WR 340 waveguide used for compensation in the L.O. line. The four nanosecond resultant pulse confirms the predicted value mentioned earlier in Subsection 2.6. As anticipated, the lower frequency components are delayed by a greater factor than the higher frequency components.

Input Pulse

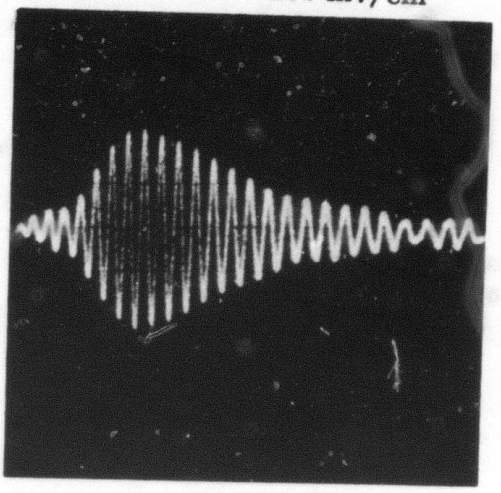
f_o = 2.4 GHz 1 us/cm 100 mv/cm



a.

Dispersed Pulse Through Waveguide

f_o = 2.4 GHz 1 us/cm 100 mv/cm



b.

Figure 3.40 Short Pulse Tester I/P & O/P

SECTION 4
VENDOR SUPPLIED COMPONENTS (PERFORMANCE AND TEST DATA)

4.1 Description and Theory of Operation

4.1.1 Wideband Radar Front End (WRFE) Transmit Channel

Description. The purpose of the WRFE transmit channel is to translate input signals at 45 ±1.25 MHz to an output frequency in the range of 3.1 to 3.6 GHz. Frequency translation is accomplished by a double upconversion process which is described in more detail in the following section.

In addition to frequency translation, the WRFE transmit channel also provides amplification of the input signal level of +10 dbm to an output signal level of +13 dbm. The interface of the WRFE transmit channel with other Wideband Pulse Compression Radar (WPCR) equipment is shown in Figure 4.1. The WRFE transmit output signal is used to drive the Transmitter Exciter, which provides additional signal amplification to an output level of 6 kw. Finally, the Exciter output signal is used to drive the high power Transmitter, which generates a peak power of 10 MW.

Theory of Operation. The block diagram of the WRFE transmit channel is shown in Figure 4.2. The design has considered all possible sources of distortion in the form of either spurious generation of undesired frequencies, and/or phase and amplitude ripple (with corresponding time side lobe generation). All interface ports have been carefully matched using either isolation or attenuation techniques. In addition, all critical broadband (500-MHz bandwidth) components have been designed and constructed to achieve the previously stated objectives. These components include the 950/3350 MHz upconverter, the 3.1 to 3.6 GHz bandpass filter, and the 3.1 to 3.6 GHz preamplifier and postamplifier units. The 950-MHz bandpass filter has also been developed to satisfy the stringent transmission/rejection characteristics listed in paragraph 4.1.4. Examination of Figure 4.2 reveals that the interface ports J1, J6 and J7 (which provide input signals to the two upconverters) are padded with either 3-, 6-, or 10-db attenuators for the following reasons:

- To decrease the LO input signal to obtain optimum drive level
- To decrease the RF input signal to a level 10-db lower than the LO drive, thereby minimizing possible spurious (harmonic, intermodulation, and cross-modulation) effects
- To reduce the VSWR of the upconverter ports to acceptable levels
- To reduce reflection interaction effects, thereby minimizing possible phase and amplitude ripple effects

The bandpass filters are provided in the upconverter output circuits to pass the desired transmission frequencies, while ensuring that all undesired spurious frequencies are rejected. The filter rejection bands include the upconverter RF input and LO frequencies, as well as the image frequency.

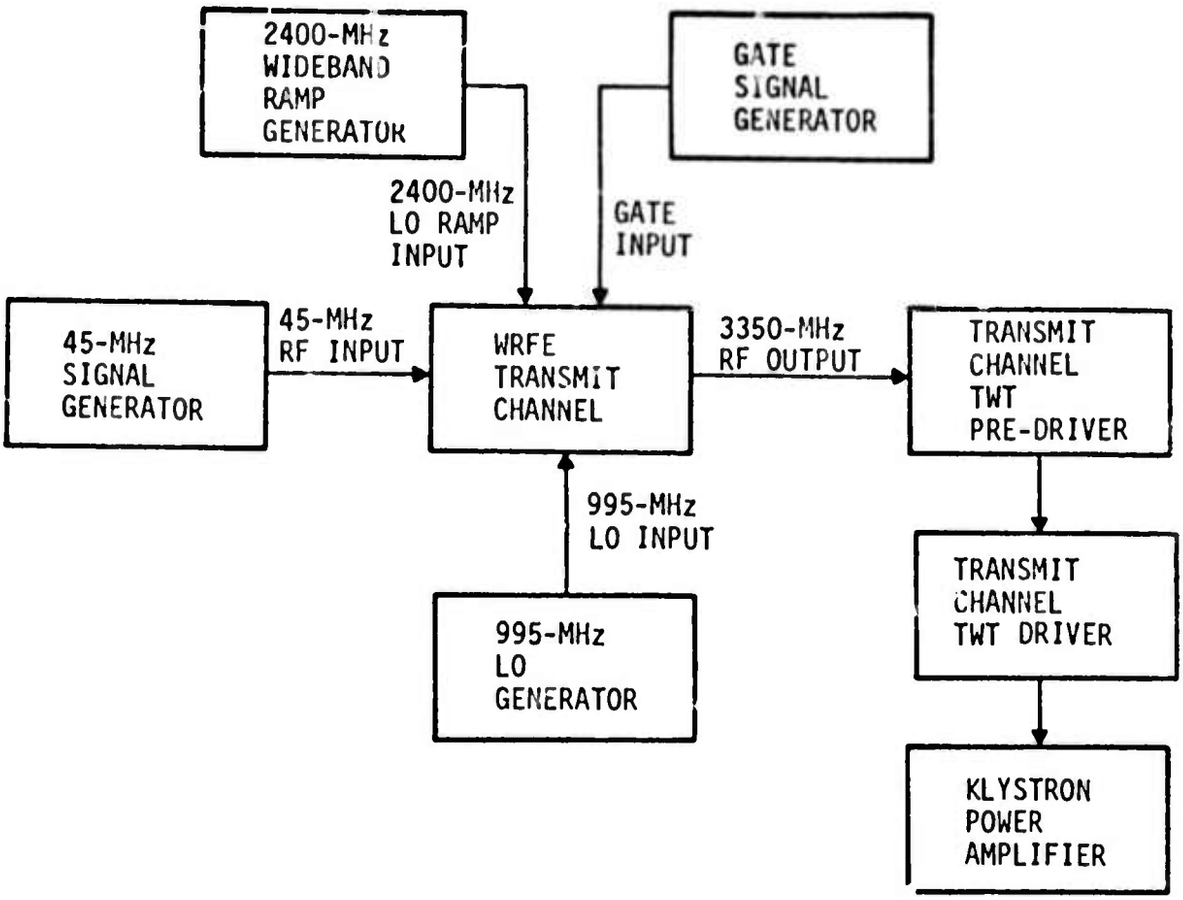


Figure 4.1 WRFE Transmit Channel, Interface Diagram

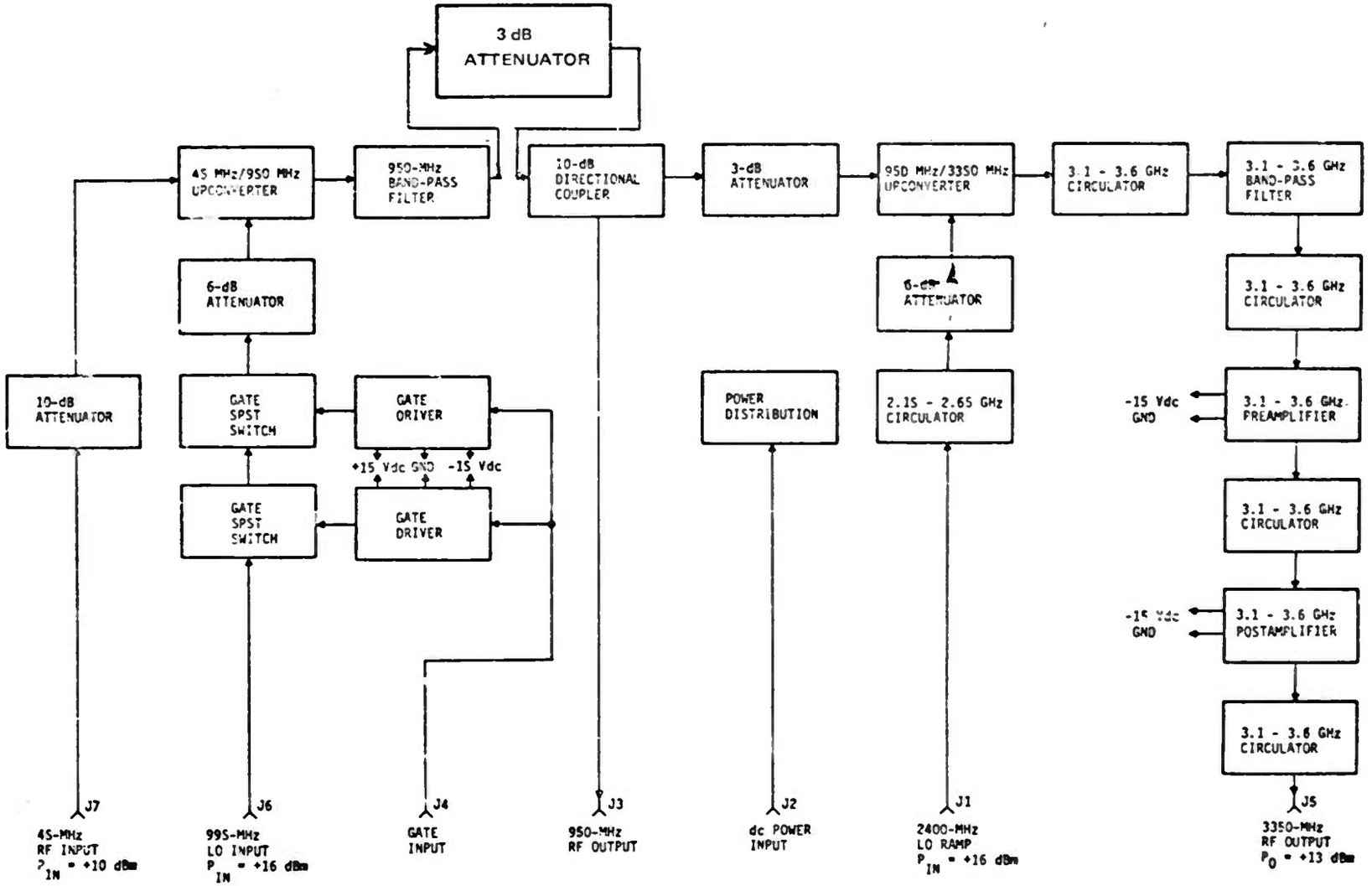


Figure 4.2 WRFE Transmit Channel, Block Diagram

The following undesired signals are effectively rejected by the bandpass filters.

a. 950 MHZ BANDPASS FILTER

(1) RF input signal at 45 MHz
(2) LO input signal at 995 MHz
(3) Image frequency at 1040 MHz

b. 3.1 to 3.6 GHz BANDPASS FILTER

(1) RF input signal at 950 MHz
(2) LO Ramp input signal centered at 2400 MHz
(3) Image signal centered at 1450 MHz

The attenuators and/or circulators shown in the main signal transmission path (between the RF input and output ports at J7 and J5, respectively) are provided to match interfacing microwave components. The resultant decrease in VSWR is a prime design consideration, since the minimization of reflection interaction effects is necessary in order to minimize distortion due to phase and amplitude ripple effects.

The gate switch has been installed in a secondary signal path (between the LO input at J6 and the 950-MHz upconverter). In this position, the gate switch functions effectively to permit main signal path transmission upon command (gate input signal at J4) with little effect on the main signal distortion properties.

The preamplifiers and postamplifiers shown in the main signal path are required to overcome a circuit loss of approximately 28 db, in addition to providing an overall gain of 3.0 db at an unsaturated output power level of +13 dbm.

4.1.2 WRFE Receive Channels

Description. The purpose of the WRFE receive channels is to translate input target signals in the frequency range of 3.1 to 3.6 GHz to an IF output frequency of 950 $\pm$1.25 MHz. In addition, amplification is provided to overcome circuit losses to provide equal input and output signal levels ranging from -85 to -40 dbm. The WRFE receive channels contain two identical subsystems, and have been designed to provide output signal levels that are matched within 1 db. The system transmits vertically polarized signals and, by time multiplexing, can receive either vertically or horizontally polarized returns. The prime receive mode is vertical polarization. However, under certain conditions where the return signal has been reoriented, horizontal polarization on receive may be better. Thus two channels are required for this polarization diversity. The interface of the WRFE receive channels with other WPCR equipment is shown in Figure 4.3 The input signal to each WRFE receive channel is supplied by an S-band transistor amplifier, which is preceded by the waveguide duplexer/limiter structures. The output signal from each WRFE receive channel is connected to a 950-MHz transistor amplifier, which is followed by the signal processing equipment.

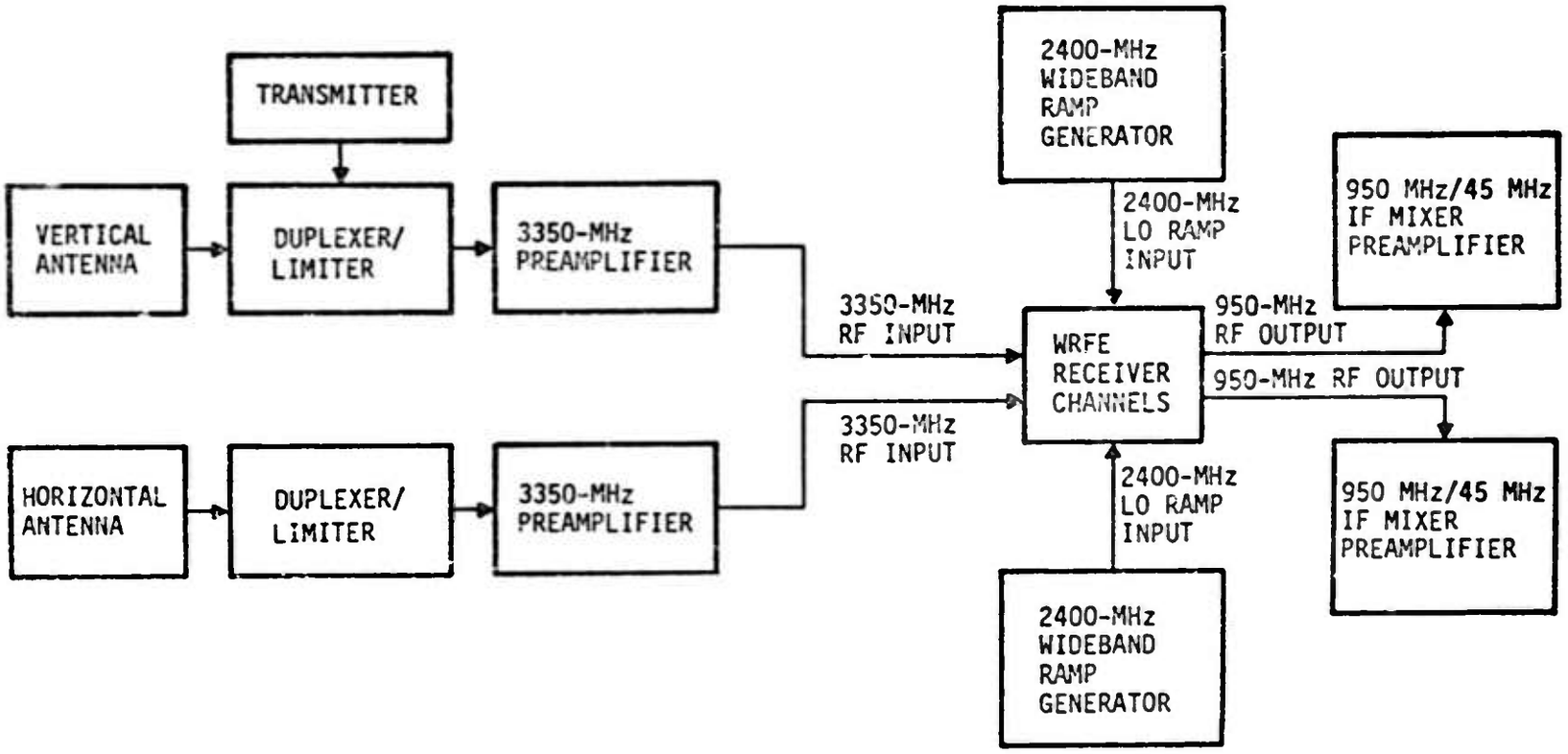


Figure 4.3 WRFE Receive Channels, Interface Diagram

Theory of Operation. The block diagram of the WRFE receive channels is shown in Figure 4.4. The same design considerations described with respect to the WRFE transmit channel have been adhered to in the development of the dual matched receive channels. Only the differences in design considerations will be presented in this section.

Interface port matching has been accomplished with an input and output circulator in the main signal transmission path between connectors J3 and J5, respectively, for receiver channel No. 1 and J9 and J7 for receiver channel No. 2. Secondary path LO signal input matching has been accomplished with a 3-db attenuator between J4 and J8, and the corresponding downconverters. The attenuator also establishes the optimum LO drive level at the downconverter LO port.

The 950-MHz bandpass filter is used to pass the desired 950-MHz signal while rejecting the following undesired signals:

- o RF input signal centered at 3350 MHz
- o LO input signal centered at 2400 MHz
- o Image output signal centered at 5750 MHz

A 950-MHz postamplifier has been provided to overcome main signal path losses of 10.8 db. An overall receiver gain of 4.0 db will be available at an unsaturated output power level as high as 0 dbm, in order to permit the observation of close test targets.

4.1.3 Equipment Installation

The WRFE equipment is installed in 19-inch racks located in the tower room adjacent to the high power transmitter. The front panels of the WRFE equipment have been designed with quick-disconnect fasteners to facilitate removing the panels in order to provide convenient access to interface connections and/or subassembly components. Interface connectors are all mounted on a horizontal flange located in the rear of the WRFE chassis in order to expedite cable hookup from the front of the rack.

4.1.4 Interface Specifications

WRFE Transmit Channel

Input Requirements

Signal	Frequency	Level
RF Input	45 MHz (2.5-MHz ramp)	+10 dbm
LO Input	995 MHz	+16 dbm
LO Ramp Input	2400 MHz (500-MHz ramp)	+16 dbm
Gate Input 2.	40 us pulse, +4 Vpk	

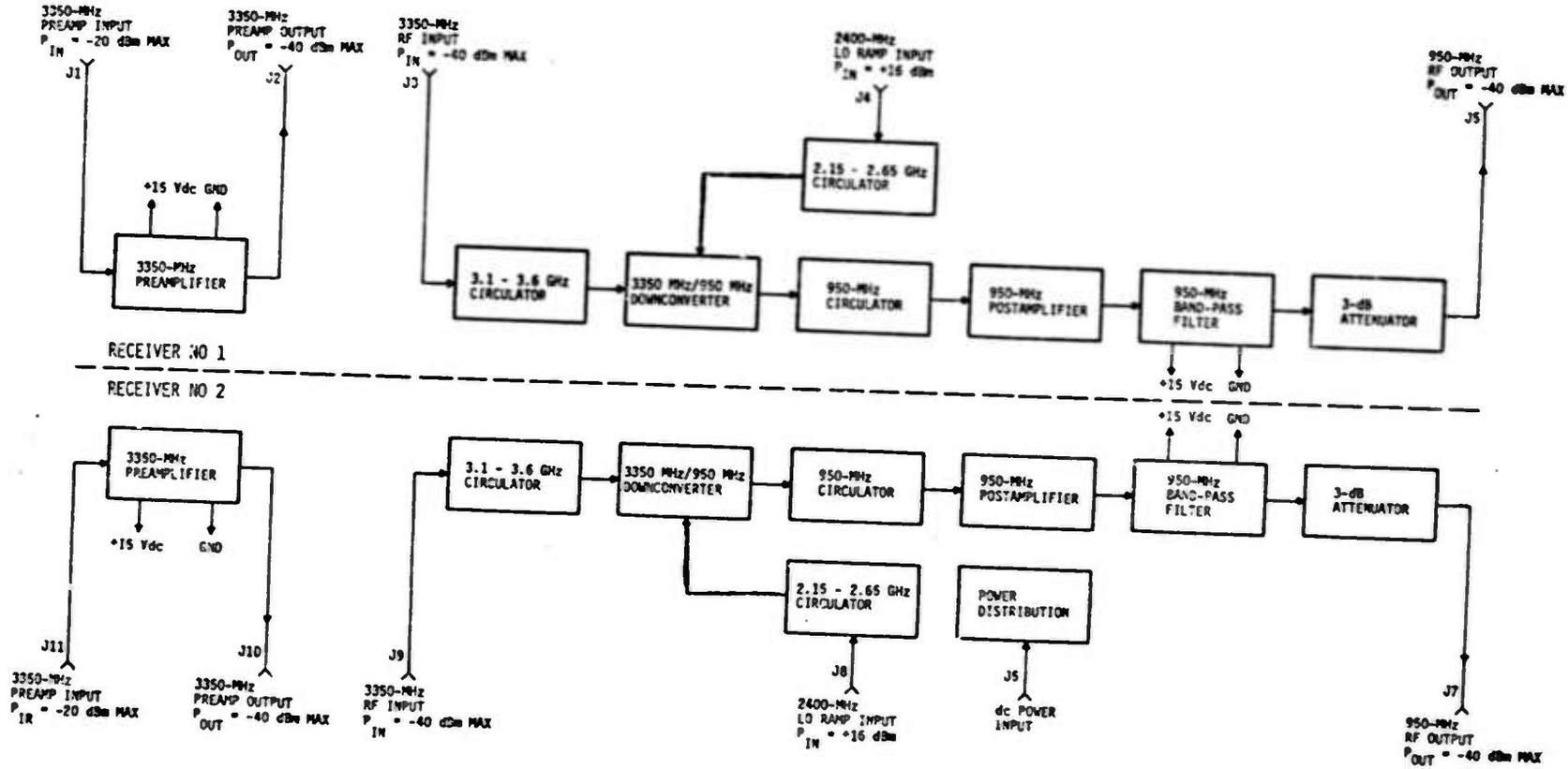


Figure 4.4 WRFE Receive Channels, Block Diagram

Input/Output Characteristics

VSWR: 1:22 max at all interface ports

RF Output Power Level: +13 dbm

RF Output Frequency: 3350 ±250 MHz (with 500-MHz LO ramp input)

Noise and Spurious Level: 50 db min rejection

Phase Ripple: ±1.0 degree periodic

Amplitude Ripple: ±0.2 db periodic

WRFE Receive Channels

Input Requirements

Signal	Frequency	Level
RF Input	3350 ±250 MHz	-40 dbm max
LO Ramp Input	2400 MHz (500-MHz ramp)	+16 dbm

Input/Output Characteristics

VSWR: 1.22 max at all interface ports

Output Power Level: -40 dbm min

Output Frequency: 950 MHz

Dynamic Range: 55 dbm min

Noise Figure: 11.5 db max*

Phase Ripple: ±1.0 degree periodic

Amplitude Ripple: 0.2 db periodic

Amplitude Match: 1.0 db max, deviation

---

* Computed receiver noise figure which will degrade the noise figure of the preamplifier that precedes the front end by less than 0.2 dB when the preamplifier has a noise figure of 6 dB and a gain of 20 dB.

4.1.5 Power Connections

The following power connections are required at the D.C. Power Input connector of each chassis (J2 for Transmit Channel, and J6 for Receive Channels):

Voltage Vdc	Current* Transmit	Receive	Pin Number
0 (ground)	114 mA dc	25 mA dc	A
-15	150 mA dc	25 mA dc	B
+15	36 mA dc	--	C
+30	--	--	D
0 (spare terminal)	--	--	F

In addition, the +4 V pk gate signal at J4 of the WRFE transmit channel must deliver a current of 160 mA dc in order to turn the gate switch on.

* Currents measured with +4V DC applied to switch.

4.2 RF Transistorized Preamplifier (MITE Q)

4.2.1 Scope

This section describes the design and operation of an RF Transistorized Preamplifier.

4.2.2 Description. The block diagram in Figure 4.5 represents the configuration employed in the design and construction of the RF transistorized preamplifier. The input signal is divided in two by means of a 90° hybrid coupler and applied to a pair of matched and balanced four-stage amplifiers optimized to cover the 3.1 to 3.6 GHz frequency range.

The outputs of both amplifiers are then combined in another 90° hybrid coupler to provide a wide-dynamic-range, low-noise signal, the gain of which has been increased by 20 db.

The equipment was tested to meet all of the following specifications at the contractor's plant and verified at site.

Center Frequency:	3350 MHz
Bandwidth:	500 MHz
Amplitude Flatness:	±0.1 db
Noise Figure:	6 db max.
Phase Linearity:	±0.6 degree
VSWR - In and Out:	1.2:1
Impedance - In and Out:	50 ohm
Gain:	20 db
Normal Input Signal Levels:	-104 dbm to -60 dbm
Matching Between Channels:	1 db amplitude ± 5 degree phase
Dynamic Range:	The overall dynamic range of the receive channels shall be 55 db defined as follows: two -60 dbm signals, either in or out of the receiver operating band, shall not generate any intermodulation or cross modulation or other spurious or noise energies within the IF passband of the receiver that exceeds -115 dbm.
Burnout Level:	The preamplifier shall withstand input signal levels of 24 dbm CW or spike energy of 10 ergs whichever is larger without physical damage to the amplifier.

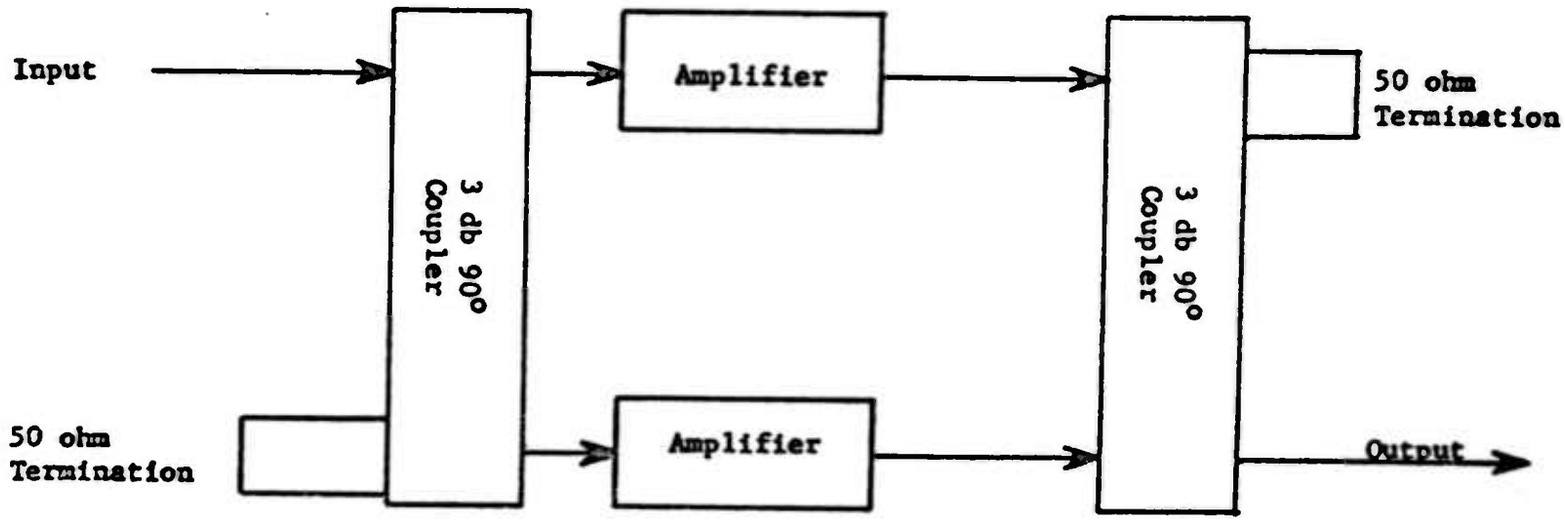


Figure 4.5 Balanced Amplifier Configuration

Available Power:	± 15 volts @ 1 amp. ± 30 volts @ 1 amp.
Operating Temperature:	+ 60°F to 90°F operating and +20°F to 90°F storage
Relative Humidity:	40% to 70%
MTBF:	1000 hours
Input & Output Connectors:	Type N

4.2.3 Theory of Operation. The following requirements have been placed on the performance of the transistorized amplifier: (1) +24 dbm burnout level, (2) 55db dynamic range, (3) 1.2/1 VSWR, and (4) 6 db noise figure. These severe requirements have led to the selection of a design approach which uses a pair of matched 90° couplers and amplifiers in a balanced amplifier configuration.

1) The burnout level was increased by a factor of two to one over a standard single amplifier. This extra margin of protection is obtained because the input signal is split by 3db so that the power level of spikes, as well as cw to each amplifier, is reduced by one-half.

2) The dynamic range is extended by at least 3db since the output level for 1db compression is, in effect, that of two stages in parallel.

3) and 4) The use of the balanced configuration with 90° couplers affords the achievement of minimum VSWR with minimum noise figure degradation. This is possible since the VSWR is not a function of the individual amplifier impedance, but rather of the similarity of the impedances of the two units. It is, therefore, possible to optimize the amplifiers for noise figure and gain and then achieve the specified VSWR by minor adjustments to achieve similarity of impedance. The power loss in the coupler is approximately 0.2 to 0.3db in this configuration, compared to about 0.5db had a ferrite isolator been used to achieve the same VSWR.

4.2.4 Alignment and Test. The final sequence for alignment of the amplifiers is as follows:

1) Tune the amplifiers for 22 db gain ± 1 db over the full 2-4 GHz frequency range.

2) Optimize the amplifiers for equal and flat (±0.25 db) gain over the 2.8 ± 3.9 GHz frequency range.

3) Measure input characteristics and select most similar amplifiers for each pair.

4) Match the amplitude and phase response of each pair of amplifiers to ±0.2 db amplitude and ±0.5° phase.

5) Check the couplers for amplitude, phase, and VSWR.

6) Assemble complete units and trim for flat amplitude and phase response.

7) Check and adjust input and output VSWR.

8) Recheck amplitude and phase response.

The schematic diagram for the final amplifier is shown in Figure 4.6.

4.2.5 Installation and Operation. There are no special maintenance requirements for the amplifier. However, since the unit is sensitive to power supply variation it is advisable to check the dc voltage at the filter terminal on the individual amplifier chain on a periodic basis. The potentiometers can be used to make small system adjustments in gain and phase if desired (1 db/volt and 2°/volt).

4.3 Pulse Compression System (Creative Electric)

4.3.1 Scope

This section describes the design and generation of a pulse expansion and compression network. This network provides a dispersed pulse 42 microseconds long with a 25-MHz bandwidth at 45 MHz (transmit pulse) and compresses or correlates the same pulse at receive time (receive pulse). The output is time-domain weighted and peak signal gain is 10 db.

4.3.2 Description and Theory of Operation

For the purpose of discussion, the system is divided into two sub-systems: 1) transmit pulse generation (sweep generation) and 2) receive pulse generation (correlation).

4.3.3 Transmit Pulse Generation. Referring to the block diagram in Figure 4.7, it can be seen that the transmit impulse generator receives two important inputs: 1) a T^2L impulse trigger and 2) an 11.25 MHz cw signal (TTL).

The 11.25 MHz TTL signal is buffered, gated and filtered, and applied to the "L" port of a doubly-balanced mixer. The impulse gate starts coincidentally with the trigger and lasts for 20 microseconds. At the center of this 20 microsecond interval, the "X" port of the mixer is driven by a 0.4 μsec long negative going current waveform, a 0.8 μsec long positive going waveform and a second 0.4 μsec long negative current waveform. This generates a pseudo-sine "X" over "X" waveform at the "R" port of the mixer.

In addition, three other current pulses of variable position, width, and amplitude are inserted into the "X" port of the mixer for optimizing the generated impulse. These signals are termed the "pre-transmit distortion compensator" and are adjusted as necessary, after the entire system has been aligned.

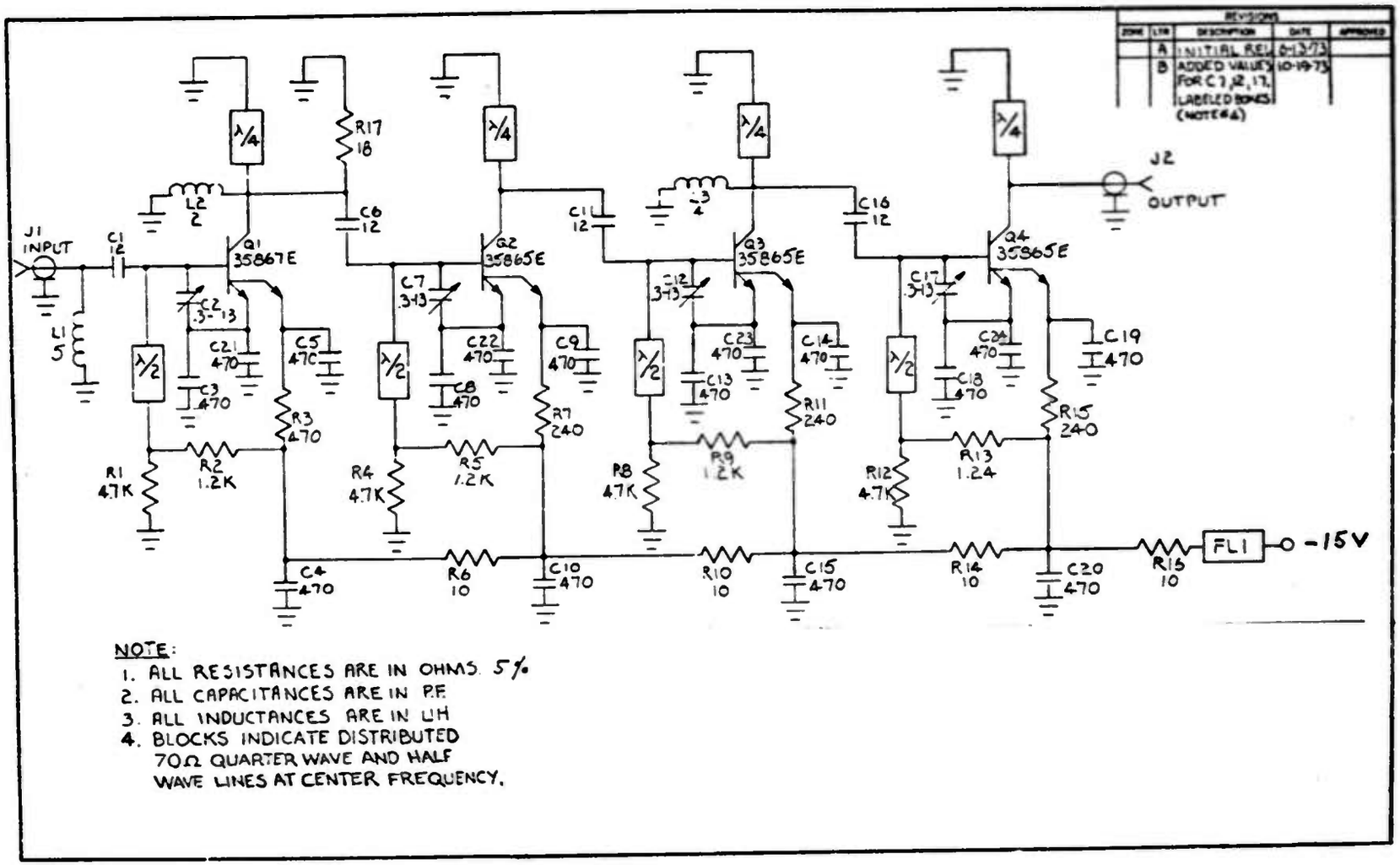


Figure 4.6 RF Transistorized Pre-Amplifier

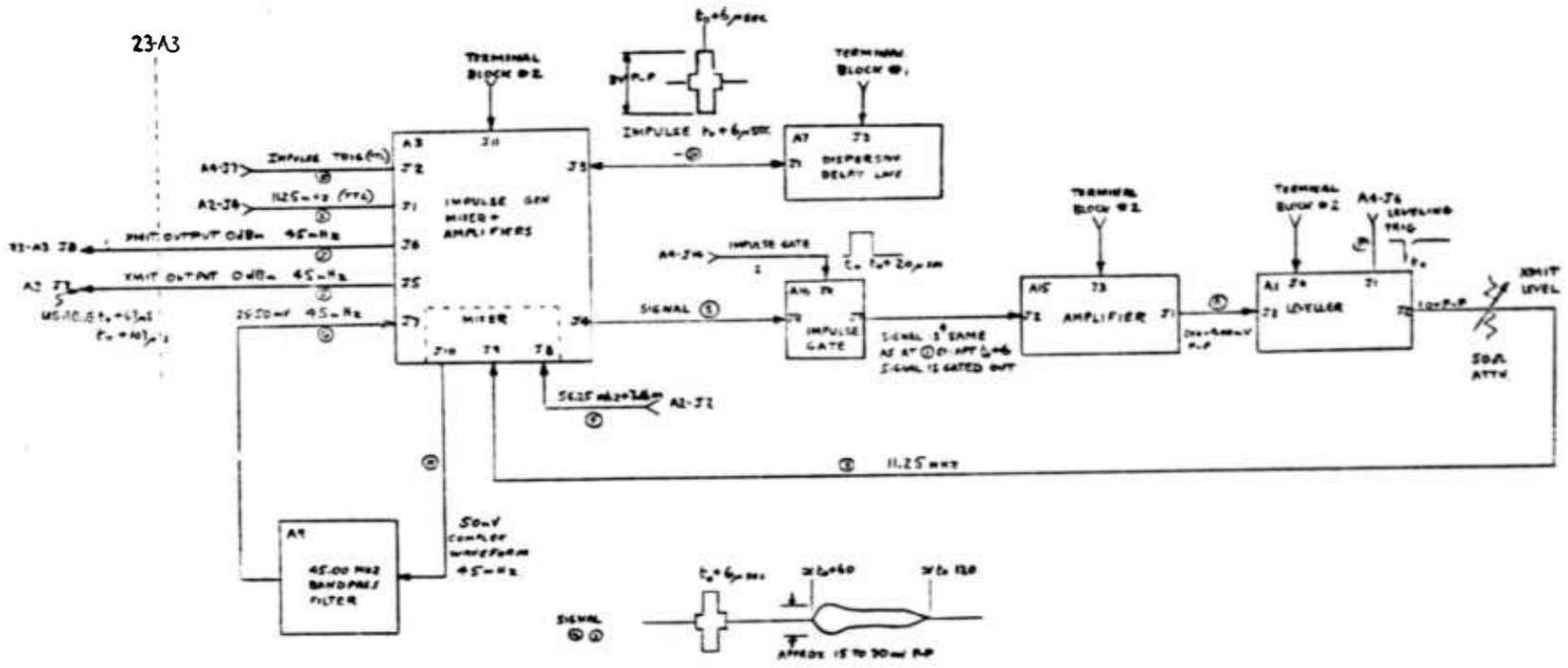


Figure 4.7 Block Diagram of Pulse Compression System 23-A3 (Transmit Pulse Generator)

The signal above is fed to a gated power amplifier where it is amplified to a level of 8 to 12 volts peak-to-peak, and then applied to the input of a single terminal dispersive delay line. Also at the input to the delay line is a pin diode switch or gate which lets the signal through during impulsing, and allows it to leave the delay line after the dispersion period. The net result has the effect of a transmit/receive switch and permits the construction of the line using only one transducer, reducing the insertion loss to approximately one half of that of the conventional arrangement.

The output of the delay line and amplifier is an unlevelled signal, about 60 microseconds long starting 60 μseconds after t_o and about 300 millivolts in amplitude. Leveling of the 11.25 MHz dispersed signal is accomplished by processing the output of the delay line in a linear amplifier having a time variant gain characteristic.

The linear amplifier contains a Schottky diode variable attenuator, and several stages of fixed gain. When the leveller is triggered on, a one-shot multivibrator delays action for 67 μsecs and a free running oscillator initiates and counts out 40 pulses and stops. The counter drives a 40 input analog multiplexer which scans the settings of 40 potentiometers which are set individually in time to adjust the output level at each of 40 one microsecond segments of the output pulse. The waveform is levelled to a final amplitude of 1 volt peak to peak.

From there the 11.25 MHz levelled signal is converted to 45 MHz center frequency with the desired chirp sense by mixing with a phase-locked 56.25 MHz signal.

4.3.4 Receive Pulse Generation (Correlation). The input to the correlator is a delayed replica of a transmitted pulse, but containing information concerning a target from which it was reflected.

Figure 4.8 will be used in the discussion on the operation of the correlator. A trigger from the synchronizer allows the 45 MHz received signal to arrive at the input to the correlator some 3 microseconds delayed in time. The input signal is attenuated by 6 db to optimize the first mixer operation which translates the signal down to 11.25 MHz by mixing with 33.25 MHz to preserve the chirp sense and provide a match for the 11.25 MHz delay line used in the correlation process.

After amplification, the received 11.25 MHz signal is fed to the weighting filter (generator). The operation of the weighting filter is similar to that of the levelling amplifier used in the transmit pulse generator described above with two exceptions:

1) Pin diodes are used instead of Schottky diodes as the attenuating element due to their wider dynamic range.

2) The time delay before processing starts is three microseconds instead of the 67 microseconds used in transmit pulse generation.

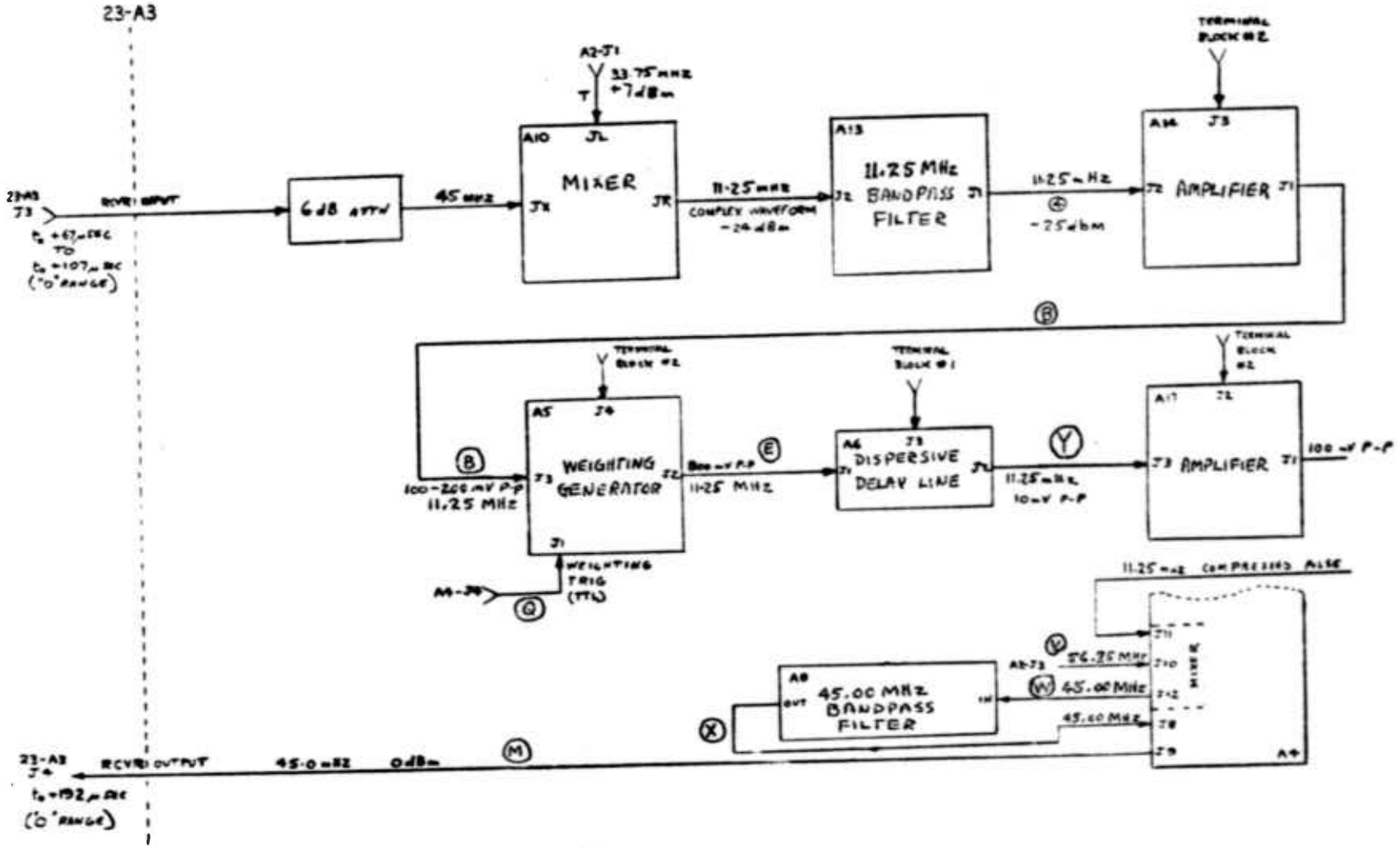


Figure 4.8 Block Diagram of Pulse Compression System (Correlator), 23-A3

The weighting filter consists of a similar number of voltage potentiometers, each gated on for 1 microsecond and adjusted to a cosine on a pedestal response with a pedestal ratio of 0.08, typical of a modified Hamming weighting.

The weighted and amplified signal is then fed to a delay line which has the property of delaying the higher frequency components less than the lower frequency components, resulting in a pulse having a constant frequeney and compressed in time to a width of 560 nanoseconds.

When properly adjusted with a linear pulse in the input the time sidelobes associated with the output pulse are approximately 37db down with respect to the main pulse.

4.3.5 Electrical Speeifications

The main eleetrical specifications of the Pulse Compression Network are summarized below:

Transmit Output Specifications

Width - 40 μseconds (2.5MIz BW)

Slope - ±2%

Length - ±0.5 μseconds

Amplitude Response - ± 0.25db

Center Frequency - 45 MHz

Bandwidth - 5 MHz

Tolerance - 45 MHz locked to 5MHz reference

Spurious - -45 db with respect to desired signal

Receive Output Specifieations

Compressed Pulse Width - 560 nanoseconds maximum

Side Lobe Level - 37db max

Linearity - ±0.5db

Spurious - 45db with respect to desired signal

Overall Speeifications

Amplitude Deviation - ± 25db

Subsystem Delay - 170 μsee maximum

Instantaneous Dynamic Range - 50 db refereneed to a -10 dbm uncompressed input signal

Signal Separation - two signals 50 μsceonds apart shall be processed without measurable degradation

4.4 HISYNC Synchronizer - (RCA)

4.4.1 General

The Test Facility High Speed Synchronizer Logic hereupon referred to as HISYNC derives the critical timing signals for the test facility radar in FM modes of operation. HISYNC is divided logically into two sections, a high speed logic section, located on a printed circuit card called Z_1, and a low speed logic section. The low speed logic is contained in two wire wrap boards Z_2, which has most of the transmit timing, and Z_3 devoted mostly to receive timing.

In addition, HISYNC contains a -5.2 volt power supply and a times 64 frequency multiplier. +5 Volts and +15 volts are obtained from the radar system. HISYNC also requires 120 volts AC for the -5.2 volt power supply. The 120 volts is obtained via connector J1 and the +5 and +15 volts via connector J2. Multi-pin connector J3 carries the digital signals between HISYNC and the existing radar synchronizer. The site 5MHz reference sine wave is connected to J4. The FM LO output is obtained from TWINEX BNC connector J5. The transmit/receive Impulse Trigger is obtained from J6, the Early Gate from J7 and the Late Gate from J8.

4.4.2 Design Details

Frequency Multiplier (X64)

The times 64 frequency multiplier is a phased-lock loop-type multiplier. It accepts the site 5 MHz reference sine wave from HP frequency standard and produces a 320 MHz signal which is used as the master timing clock. The high-speed logic in HISYNC develops a synchronous 5 MHz square-wave from the 320 MHz which is used by the multiplier to compare against the 5MHz site signal and thus produce a phase-locked 320 MHz. The consequence of this is that the 320 MHz and 5 MHz square-wave are coherent with the site reference.

System Block Diagram

Figure 4.9 shows the HISYNC Block Diagram.

High Frequency Section

Clock Driver. The 320 MHz sine wave is shaped by an ECL level 50-ohm line driver. This develops the 320 MHz clock signal which drives the clock inputs of four high speed flip-flops. An alternate or "back-up" driver system is also included. In the event that this is used, the input ECL driver and terminating resistors are removed and replaced with a resistor of 51 ohms. The 320MHz signal is then fed into the alternate driver and coupled via a .01 μF capacitor. In either case, the logic performs identically.

Two Phase Clock Generator. A binary divider produces the main 160 MHz clock. Three additional flip-flops are used to develop the 2^3 bit of fast timing. These flip-flops U2, U3 and U4 shown on Figure 4.11 develop 160 MHz at either polarity 0° or 180° depending upon the input signal at the 2^3 CLK Mode line. When the 2^3 CLK input is low the signal at U4 Q-output is 160MHz at phase 0°, the same as at U1 Q-output. When the 2^3 CLK input is high the

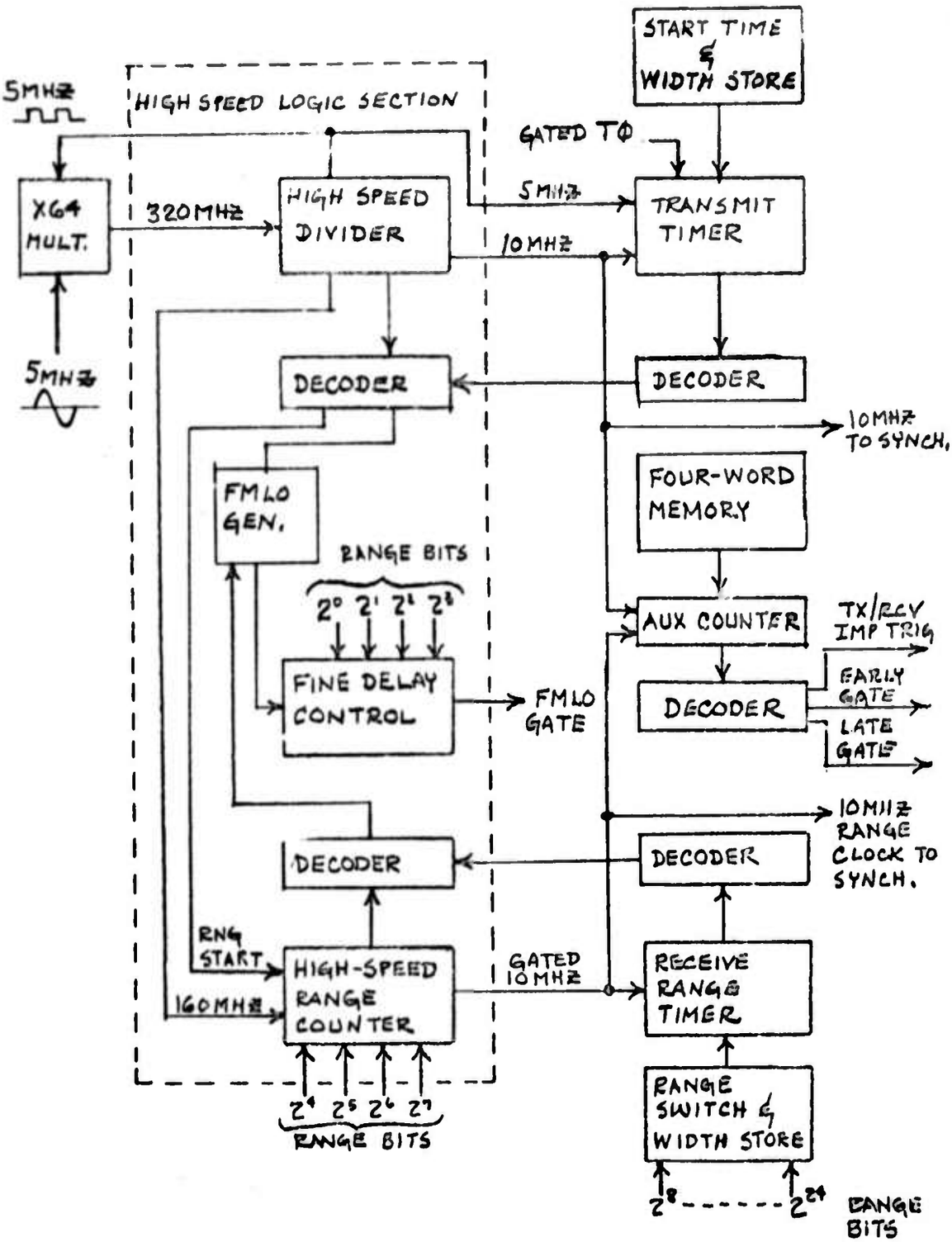


Figure 4.9 HILSYNC System Block Diagram

signal at U4 output is 160MHz at 180° or opposite polarity to the main 160MHz clock at U1 Q-output. This reversal in polarity will be used as the 2^3 bit of receive time delay or equivalent to 3.125 nseconds $\left(\frac{1}{320\ \text{MHz}}\right)$.

The logic design shown in Figure 4.11 was adopted following rejection of the standard technique shown below. To perform logical functions, gates are normally used; however, the time delay of the signal through the gate to perform the logic function will slow down the overall operation. It is therefore necessary to conceive a method of eliminating the gates' delay while obtaining a clock at half the frequency of the reference clock that will move in the basic increment of the reference clock. Figure 4.10 shows the implementation of this circuit if gates were used and if high frequency operation were not a consideration.

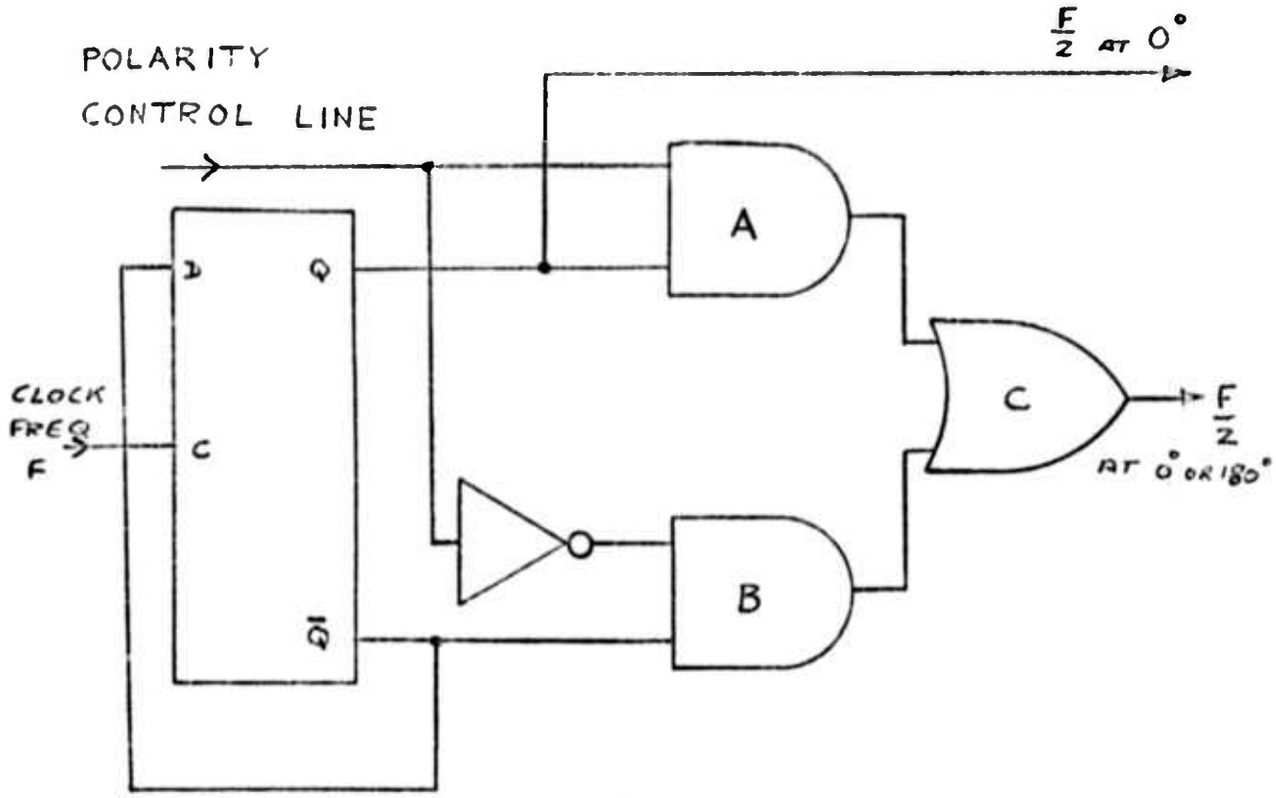
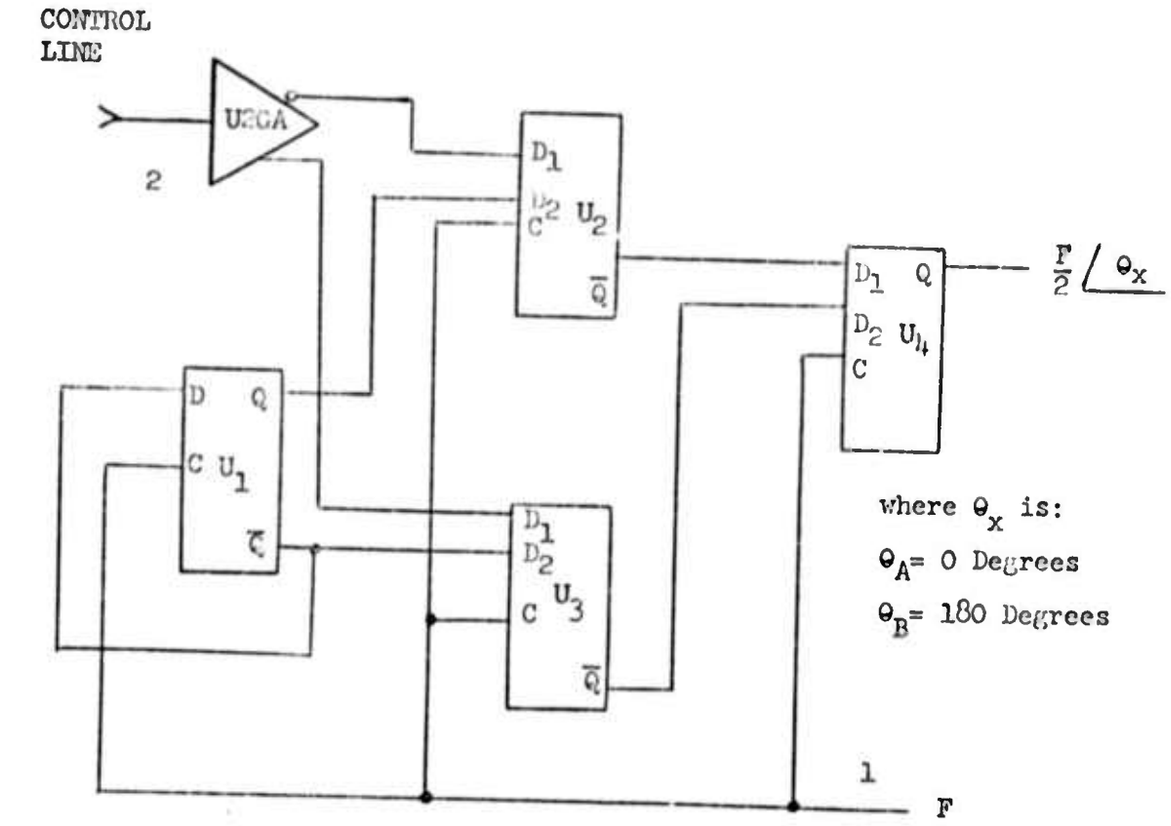


FIGURE 4.10 - EQUIVALENT CIRCUIT SHOWN USING GATES WITH NO REGARD FOR DELAY.



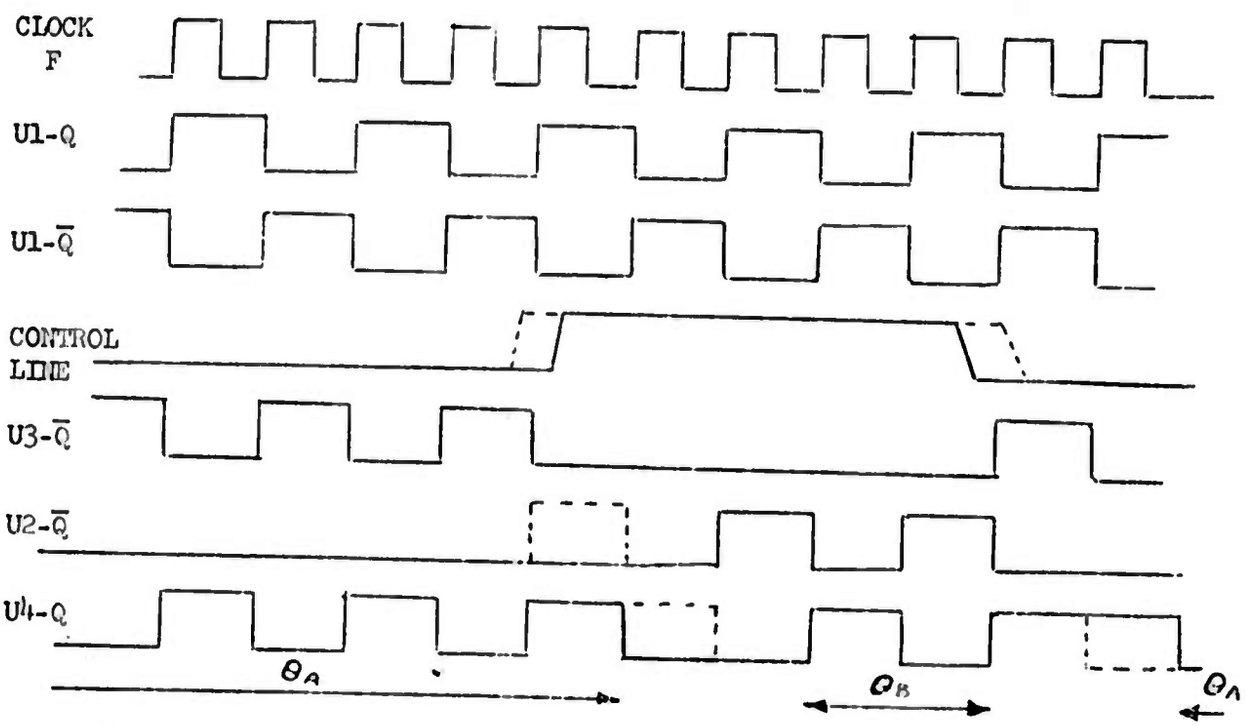


FIGURE 4.11 HIGH-SPEED TWO-PHASE CLOCK GENERATOR

It should be appreciated that if the signal out of OR Gate C were used as the clock frequency for other counting circuits, the other counters may be operated at increments of the period of frequency F by adjustment of the control line. The drawback of this logical arrangement is the delay. For example, the precision desired between phases from OR Gate C must be within 100 picoseconds (0.1 nanosecond), then the differential delays between AND Gates A and B and the Q and $\overline{Q}$ outputs must also cumulatively be within 100 picoseconds. Since this is impossible to guarantee, the circuit is useless for this precision.

In Figure 4.11 the preferred design operates as follows: Three flip-flops U1, U2, U3 and U4 are shown, all with their clock inputs connected to common line 1. The flip-flops shown feature two D-inputs where the signals applied to the D-inputs are logically ORed by the flip-flop. Flip-flop U1 is connected as a binary divider with its $\overline{Q}$-output connected to its D-inputs. Flip-flop U2 has one D input connected to the Q-output of flip-flop U1 and the other D-input connected to the complement of control line 2 via Gate U26A. Flip-flop U3 has one D-input connected to the $\overline{Q}$-output of flip-flop U1 and the other D-input connected to control line 2 via the output of Gate U26A. In this manner, either flip-flop U2 or U3 is turned on. If the control line is high the D1-input of flip-flop U2 will be low and flip-flop U2 will be able to respond to signals on the D2-input. At the same time the D1-input of flip-flop U3 will be high causing the Q side of flip-flop U3 to be continually high no matter what happens on its D2-input. The $\overline{Q}$-output of flip-flop U3 will be low. If the control line polarity is reversed or made low then flip-flop U2 Q-output will be forced high its $\overline{Q}$-output remaining low and flip-flop U3 will be allowed to operate or respond to the signal on its D2-input.

Flip-flop U4 has one D-input connected to the $\overline{Q}$-output of flip-flop U2 and its second D-input connected to the $\overline{Q}$-output of flip-flop U3. Thus, there are three shift register stages in tandem U1, U2, U4 or U1, U3, U4 depending on the state of the control line. If control line 2 is high the shift register is made up of U1U2U4, U2 indicating its $\overline{Q}$ output is used. If control line 2 is low the shift register is made up of $\overline{U_1 U_3} U4$.

The polarity of the signal available at the Q-output of U4 is thus dependent on the control line. If the control line is low the signal at the output of flip-flop U4 will be in phase with the reference signal at flip-flop U1 Q-output. If the control line is high the signal at the output of flip-flop U4 will be out of phase with the reference signal. Figure 4-11 shows the timing waveforms.

The control line normally is set during the system "dead" time (shortly before the REC FM LO) so there is no conflict with the switching time of the control line as shown dotted in Figure 4-11.

Main 10MHz and 5MHz Timer. Four flip-flops are connected as a binary up-counter dividing the 160 MHz reference clock by 16 thus producing the 10 MHz CW clock for the low speed logic. The last three stages of the four stage counters are decoded and applied to the two D-inputs of a flip-flop. The decode of the first stage output is obtained by applying it to a clock input of the same flip-flop with the 160 MHz applied to the other clock input. This produces a 5 MHz square wave which is coherent with the 160MHz clock. Tests have shown that the jitter between the input 320MHz and the output 5MHz is virtually nonexistent (< 20 psec.). Therefore, the 5 MHz signal is essentially coherent with the 320 MHz clock. The 5 MHz is made available as a balanced output signal which is sent over balanced 100 ohm shielded cable to the multiplier. The 5 MHz is also used by the low speed logic to aid in establishing a reference sync signal.

Range Counter Start. The 10 MHz clock obtained from the 10 MHz Timer is sent to the low speed logic via a level converter (ECL to TTL). The low speed logic determines at which time the range timer should start (approximately TØ time) and sends back a signal derived from the 10MHz. This signal is converted from TTL level to ECL where it is further decoded by sensing the all one's count of the 4-stage 10 MHz timer. The sensing of the "all-one's" state of an up-counter allows for error-free detection no matter how many stages in the counter. This is because the last stage in the chain is the first stage to reach the terminal one's count.

The decoded output is now a positive pulse 6-1/4 nanoseconds wide occurring at range start time. It is applied to the D-input of another flip-flop which is also clocked by the reference 160 MHz. Consequently, at the next 160MHz clock pulse the $\bar{Q}$-output of the flip-flop will go low. It is immediately fed back to its own D-input via an inverting gate and a "wired-OR" connection to the 6-$\frac{1}{4}$ ns pulse. This locks the D-input high so that the flip-flop will not return to the zero state, at the next clock pulse thus producing a gate for receive timing. This condition will exist until a high level is sent to the other input of the inverting gate(RANGE STOP). RANGE STOP is actually a short pulse occurring at the beginning of TØ. Thus, this gate will allow the range counter to operate for almost the entire pulse repetition interval (1/70 sec). The negative gate from this flip-flop is the receive timer gate.

TRANSMIT FM LO. The start time of the XMIT FM LO is derived from the 10 MHz clock by the low speed logic and returned as a 0.1 μsec pulse via a level converter. The counter "all-one's" is sensed just as in RNG start. Thus, a 6-1/4 nanosecond pulse is obtained and controls the D-input of a flip-flop. Assume that the other D-input is low; this flip-flop will toggle high and then low on the next two 160MHz reference clock pulses. The 6-1/4 nsec output pulse from this flip-flop is sent through a gate. The pulse output from this gate is applied to another amplifier which is clocked from the reference phase of the two phase clock (2^3 is low during XMIT). Thus another 6-1/4 nsec pulse shifted 6-1/4 nsec from its input is obtained from this Q-output. This pulse is sent through delay line assembly Z2 on module Z1 which for XMIT is switched to zero or minimum delay. The pulse is then applied to the clock input of another flip-flop, arranged to toggle as a

binary counter. Assume that this flip-flop had been in the high state; then when the pulse arrives it will toggle to the low state and will remain this way until another pulse arrives. The next pulse to arrive represents the trailing edge of the FM LO XMIT pulse and is obtained from the low speed logic and goes through a duplication of the events just described for the start pulse. The trailing edge pulse toggles the flip-flop to the high state thus producing the desired FM LO XMIT pulse width. Shortly before the arrival of this pulse, the low speed logic sends a high level signal for correct polarity locking (POL LOCK) through a level converter and onto the other D-input of the toggled binary counter. This insures that the pulses for FM LO XMIT will always be at the same polarity. The POL LOCK signal level is dropped before receive.

FM LO POL LOCK. The FM LO Polarity Lock signal is provided for three reasons: a) to establish the correct polarity of the FM LO signal. This is necessary if it is remembered that the FM LO gate is obtained from a flip-flop toggling on an FM LO trigger. The first trigger toggles the flip-flop on (the leading edge of the FM LO Gate) and the second trigger toggles the flip-flop off (FM LO Gate Trailing edge). It is easy to lose sense wherein the leading edge becomes the trailing edge and vice versa unless a level is introduced (on the other D-input of the high speed generator flip-flop) establishing the correct polarity; b) to prevent toggling when the three least significant bits of range delay are put in or removed, the delay line sections are switched in or out and the switching transient could cause the FM LO flip-flop to toggle. By holding the control D input high during this interval a transient clock pulse will not do anything but shift the state of the flip-flop to its already correct high or "one" condition; c) to inhibit only the transmit and receive FMLO Gates when operating in the FM 2.5 MHz bandwidth mode. All other timing functions of the HI-SYNC logic are enabled.

Receive 10MHz Timer. The receive timing gate which was described in the Range Counter Start above is a negative gate and is applied to the second clock input of a flip-flop. When the gate goes negative this flip-flop is allowed to toggle from the reference 160 MHz clock. It represents the first of four stages of the range or receive counter producing a 10 MHz receive clock. It is actually the 2^4 bit of range since the first four bits are derived separately. The remaining three stages comprise the Range Delay Bits 2^4 through 2^7. All four stages are preloaded at TØ just prior to RNG START with the complement of the range word: bits 2^4 to 2^7. The gated 10 MHz thus produced is sent to the low speed logic via a level converter. Note that the phase and starting polarity are a function of the range bits 2^4 to 2^7.

REC FM LO. The low speed logic using the receive 10 MHz clock derives a pulse 0.1 μsec wide at the beginning of Rec FM LO position similarly to the way the XMIT pulse was obtained. The pulse is level converted and decoded with the "all-ones" states from the receive counter described above producing a positive 6-1/4 nsec pulse (range oriented) applied to the 2nd D-input of a flip-flop. At this time the first D-input is negative. At the next 160 MHz reference, Clock Pulse, this flip-flop goes to a high level and then to a low on the following clock pulse. The output of this flip-flop may be sent

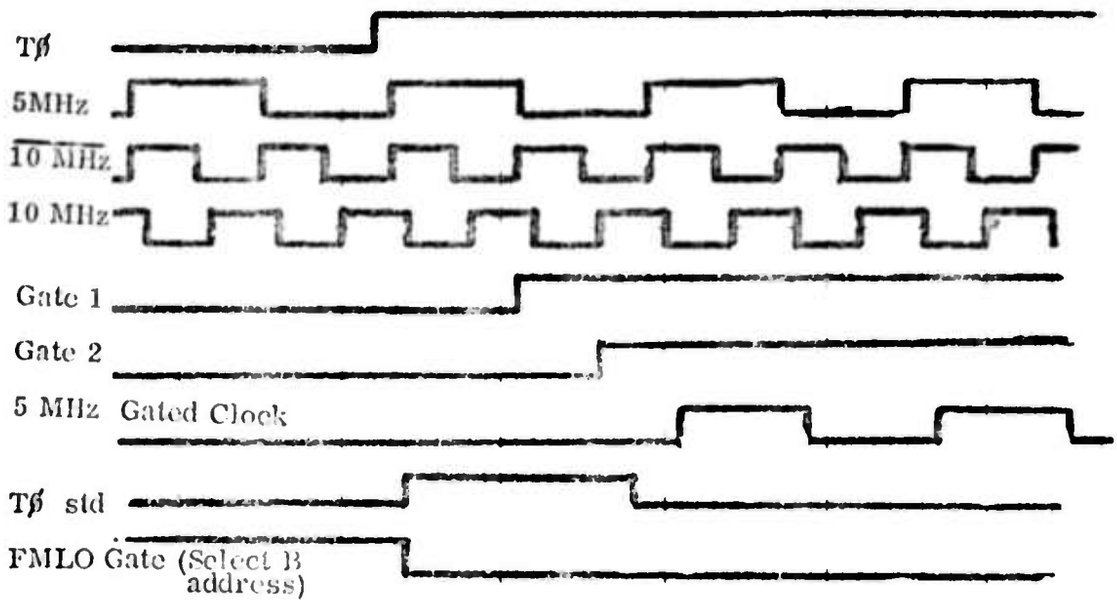
through either of two gates depending on whether the 2^3 bit of range is required. If it is not required, the pulse is treated as in XMIT and no delay is added. If the 2^3 bit of delay (3-1/8 nsec) is required, the pulse is sent thru a gate and then into the D-input of another flip-flop via a delay line DL_1. In addition, the 180 degree phase of 160 MHz clock is selected to clock this flip-flop. The out-of-phase clock causes a delay of 3-1/8 nsec in the clocking of this device. The 3-1/8 nsec delay line in the D-input insures that the data skew will be correct for proper clocking when the 2^3 bit is selected. The narrow pulse from this flip-flop is sent thru delay line assembly Z2 where additional delay may be selected.

Switched Delay Lines. The delay line assembly is a 3-bit delay system offering eight steps of delay (2^0 to 2^2 bits of range). The LSB (2^0 of range) is 390 picoseconds. The delay lines are 50 ohm microstrip lines on a thick film ceramic substrate. The hybrid contains a new "fritless" gold and wire bonded NIP diode chips. (NIP are identical to PIN diodes except the cathode and anode are reversed.) There are four diodes per delay line switch making up a double pole double throw switch. Thus, each line is independently switched in or out. The diode biases are made via 0.47 μH inductors included in the hybrid package. The push-pull switching signals are obtained from discrete transistor circuitry on the module. The NIP diode operating bias voltage levels are designed to match the input and output ECL circuit levels.

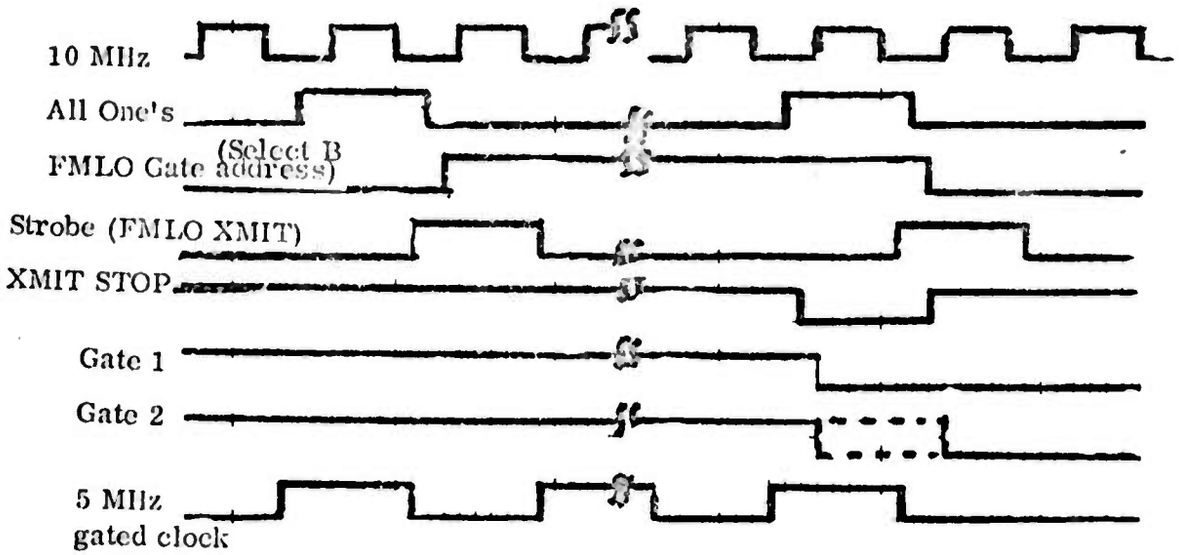
PIN diodes by nature are microwave devices. The signals through them should be faster than their recovery time. For this reason, only a narrow pulse is sent down the line, 6-1/4 nsec, rather than the FM LO pulse width which might be of 40 µsec duration. To create the FM LO pulse, therefore, two narrow pulses are sent through the line: one for start and one for stop. Another flip-flop generates the FM LO pulse by turning on the first pulse and off on the second.

Transmit Timer. The low frequency portion of the transmit timing for HISYNC is mostly contained on board Z_2. The main TØ signal from the radar is used to "steer" a flip-flop. The 5 MHz signal from Z_1 toggles the flip-flop on the next 5 MHz negative clock edge. The gate thus created, called Gate 1, is transferred to a flip-flop which is clocked from the 10 MHz clock from Z_1. This creates a gate on the negative edge of $\overline{\text{10 MHz clock}}$ or equivalent to the positive edge of 10MHz clock. This gate is called Gate 2. Gate 2 is transferred to another flip-flop which enables the binary counter function thus producing a gated 5 MHz signal which is used by the transmit timing counter, Figure 4-12.

TØ STD. A standardized TØ pulse is required for general initiation purposes. This pulse is made narrower than TØ so that after its initializing is over it will not inhibit proper operation. The pulse is created by flip-flop U1B. The leading edge of TØ clocks the flip-flop thus starting TØ STD and the leading edge of Gate 2 sets the flip-flop thus terminating TØ STD. In a CW mode of operation or in any CW PRI, the timing functions of the HISYNC must be gated off. This is accomplished by inhibiting the TØ pulse coming from the slow-speed synchronizer, thereby preventing initialization of



a) Waveforms at beginning of transmit time - Board Z2



b) Waveforms at lead and trail edge of FMLO gate

Figure 4.12 Transmit Timing Waveforms

the HISYNC logic. The 10 MHz transmit clock is not under any logic control and therefore continues to run normally. The 10 MHz receive clock is shut off for a brief interval between PRI's when the HISYNC is active in order that range delay bits 2^0 through 2^7 may be strobed into the counter. When the TØ is inhibited, the receive clock free-runs and no delay bits are strobed. As a result a range-time jump of approximately 0.1 μs can occur, but the radar system is insensitive to this deviation in non-chirp modes. See Figure 4-12.

Transmit Counter. The transmit counter performs two functions. It determines the beginning time of the FM LO transmit pulse and the width of the FM LO pulse.

The transmit counter is a programmed binary ripple-carry counter with the "all-one's" condition of each stage decoded. The counter consists of three four bit stages (12 stages total). The "all-one's" condition is detected by AND gates. The "all-one's" decode pulse is applied to a flip-flop which is clocked by the 10 MHz clock producing a strobe pulse to load the program number into the counter. The two programs: start time and width are hard-wired "Read Only Memories" (ROM). The two different programs are selected by the two-position logic switches comprising 4 poles on each of three packages. The switch position is determined by an address flip-flop. This flip-flop is connected to toggle as a binary counter or divide-by-two circuit and is initially set by TØ. The low level from the $\overline{Q}$ thus places the select switches in the "A" position which selects the FM LO start time. However, this level remains until after the FM LO gate is produced for a strobe pulse to load in the initial transmit start time. Assume, for the moment, that somehow the counter is loaded with the correct number prior to TØ. As shown in Figure 4-12(a) a gated 5 MHz clock is applied to the counter. The number previously set in and stored in the counter is equal to the one's complement of N-1 where N is the number of 0.2 μsec, pulses of delay required from the start of the 5 MHz gated clock to the start of the FM LO gate.

As the counter reaches the "all-one's" state the coincidence AND gates produce a pulse the trailing edge of which toggles the address flip-flop. See Figure 4-12(b).

The flip-flop output causes the select address B line to rise thus switching the program word from FM LO start time delay to FM LO XMIT width. At the next 10 MHz clock pulse a load strobe is generated that programs or loads the counter to the width number. The load strobe is also sent to the high speed logic on Z_1 where it is further decoded and refined and causes the beginning of the FM LO XMIT pulse in coherence with the 320 MHz clock. The number for the width is the one's complement of W-1 where W is the number of 0.2 usec increments of width desired. As an example: If the desired width is 40 usec the number set in is

$$\overline{W\text{-}1} = \frac{40}{0.2} - 1 = \overline{200\text{-}1} = \overline{199} = \overline{000011000111} = 111100111000$$

The counter has thus been reloaded "on-the-fly" and continues counting 5 MHz clock pulses.

At the next all-one's condition the counter repeats the above operations. The trailing edge of the "All-One's" pulse toggles the address flip-flop and the select B Address line falls thus placing the load switch in the position to select the XMIT start time delay. This number is loaded in by a strobe from a flip-flop toggled by 10 MHz, and steered by the "all-ones" pulse. The correct number is thus stored in the counter until the next repetition period. An XMIT STOP Trigger is also created by an AND gate which AND's the select B address gate also shown as FM LO Gate and the "All-One's" pulse. The XMIT STOP PULSE sets a flip-flop which terminates gate 1. On the next negative edge of 10 MHz clock Gate 2 is terminated. This turns off the 5 MHz gated clock and the transmit sequence is completed until the next repetition period TØ occurs.

Receive Timer. The low frequency portion of the receive timing for HISYNC is mostly contained on board Z3, as described in Subsection 4.4.1. The timer consists of a programmed counter similar to that in transmit except the first stage is a flip-flop. The remainder of the counter is made up of 16 stages, 4 bits in each of 4 logic packages. Thus, Range bits 2^8 to 2^{24} are on board Z3.

Pulse TØ loads the range word into all the counter stages. (Range bits 2^0 to 2^3 are also loaded into a four-bit storage register at this time This data will be used later to select the requested delay line and 160 MHz phase bits. Bits 2^4 to 2^7 are also loaded into the four high-speed counter stages on board Z1 by the Data Strobe line on board Z2 at TØ time). Shortly thereafter a gated 10 MHz clock is received from board Z1. The range clock or 10 MHz Rec Clock is initiated by the transmit 5 MHz gated clock. The 10 MHz Rec Clock has been further refined by high speed board Z1 so that it is synchronous with the 320 MHz clock. Range bits 2^4 to 2^7 are applied to Z1 so that the 10 MHz receive clock moves in range in $6\frac{1}{4}$ nanosecond increments.

Range Bias. A range bias may be added (or subtracted) from the range word to position the REC FM LO pulse where desired depending on overall system demands. Since the range word required by a pre-programmed up-counter is the one's complement of the range, adding a bias actually requires a subtraction. Subtraction is done with a two's complement, i.e., add the one's complement and include an input carry. Any overload carry is discarded. An input carry line is provided at the first counter stage. A four-bit example of a range addition is shown:

A bias of 5 will be added to the range word:

Input carry	1
Zero range	1111
5 = 0101, $\overline{0101}$ = +	1010
	1010

RANGE INCREMENT	RANGE WORD AS RECEIVED FROM TRACKER RANGE	COMPUTED RANGE WORD WITH BIAS OF 5
0	1111	1010
1	1110	1001
2	1101	1000
3	1100	0111
4	1011	0110
5	1010	0101
6	1001	0100
7	1000	0011
8	0111	0010
9	0110	0001
10	0101	0000
11	0100	
12	0011	
13	0010	
14	0001	
15	0000	

Counter Operation. The corrected range word is loaded into the counter by T$\emptyset$ STD. The receive counter has two pre-triggers as well as an "all-one's" decoded.

Early Gate width is also used for Late gate width. This is done by feedback connections within the address control logic.

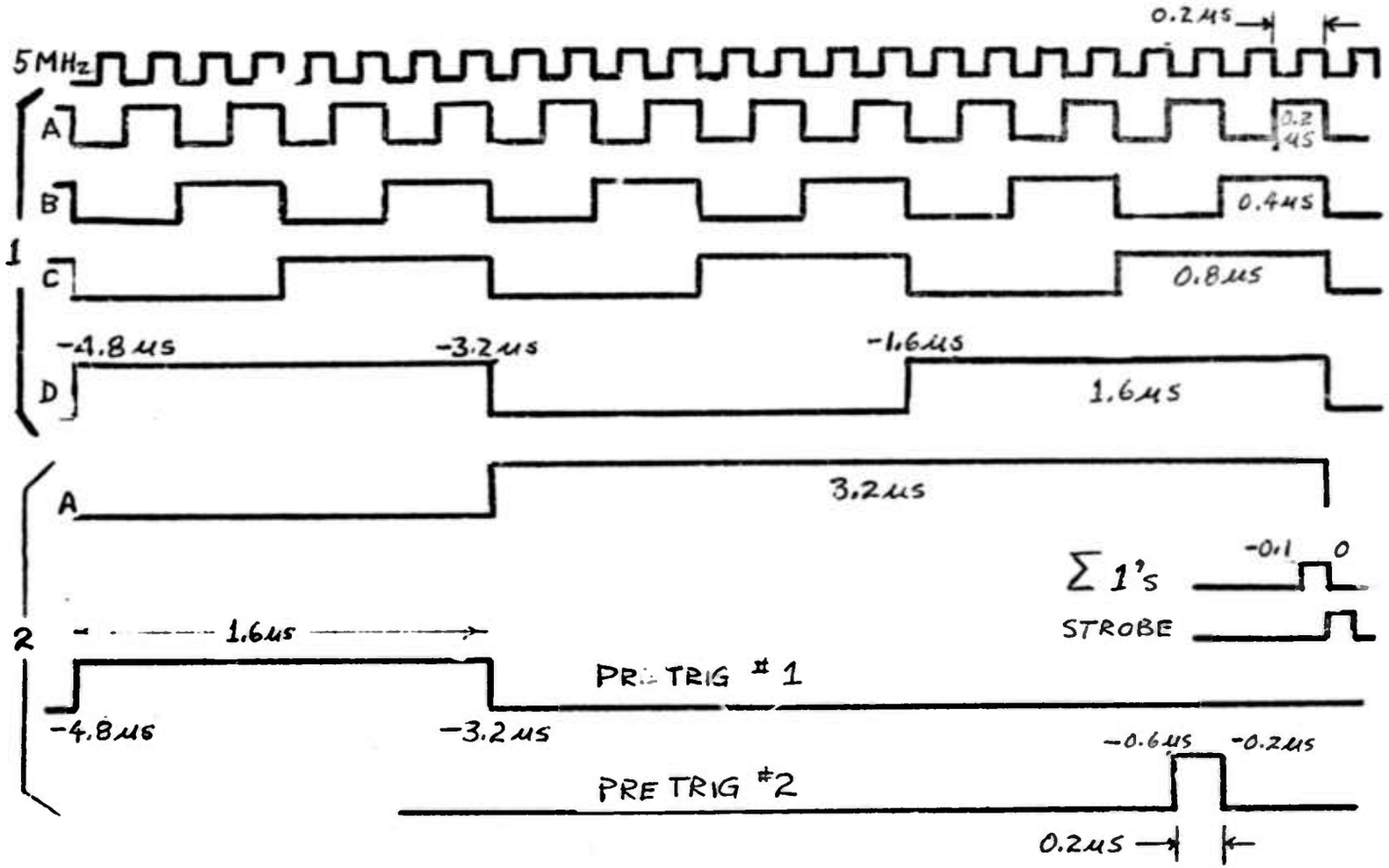


Figure 4.13 Range Pretrigger Development

The decoding waveforms are shown in Figure 4-13. The first or earliest pre-trigger is used to turn on a gate called the LSB DATA HOLD gate. This gate is used to send the least four bits of range to the high-speed logic. This gate also serves to change the word into the receive counter from FM LO range to FM LO range width so that at the next data strobe time the REC FM LO width duration will be loaded into the counter. The second pre-trigger is used to toggle the FM LO POL LOCK signal to a low and also starts a gate which will be used to allow the receive 10 MHz clock into the AUX counter. The counter "all-one's" decade initiates the generation of a reload strobe. The trailing edge of this pulse is also used to toggle a flip-flop which turns on a gate that is used to simulate the last 8 stages of the counter being in the all-one's state. This is a negative gate seen at the input to an OR gate which also receives the true 8-bit decoding. When the counter again reaches "all-one's" after counting the time interval desired for the REC FM LO pulse width, the decoded pulse initiates the toggling of two flip-flops. The gate from the latter flip-flop forces a clear on the first 4 stages of the counter so that the counter doesn't continue to generate REC FM LO gates.

AUX Counter. The AUX counter is provided to perform the auxiliary functions of generating the TX and RX IMP trigger and the Early and Late Gates. The TX and RX impulse trigger are provided on the same line. However, the TX pulse is fixed with respect to TØ while the RX pulse must move with target range. The TX pulse is positioned approximately 20 μsec from TØ while it is desirable to have the RX pulse approximately under the FM LO Receive pulse. The Early and Late gate must also move with range with their position delayed about 300 μsec from the RX pulse.

The logic to create these pulses is contained in one programmable 12-Bit counter. The programs are contained in a four-address wired "Memory" comprising six logic packages.

The address contents are listed below:

ADDRESS	CONTENTS (TIME DELAY)
0	Delay between TØ and TX IMP Trigger
1	Duration between -0.6μs range pretrigger and the RX IMP Trigger
2	Duration between the RX IMP Trigger and the beginning of the Early Gate
3	Width of the Early and Late Gates

The AUX counter is located on board Z2. The clock is derived on Z3 as is the decoding for the output pulses. The logic is broken out in a separate schematic for clarity. The counter operates first from the 10 MHz clock turned on near TØ (Gate A) and derives the TX IMP TRIG at which time gate A is turned off by Gate 2. A clock signal is not applied again until the receive pretrigger turns on gate B. This allows the Rec 10 MHz clock into the counter.

Address Counter. The address counter is used to set the memory switches so that the proper word is always loaded into the counter.

A pretrigger is decoded from the AUX counter which is used to increment the address counter. The counter is cleared at TØ so that the TX trig word is first made available to the counter. The counter is designed to count 0, 1, 2 and 3 and then stay at address 3 no matter how many times it is incremented so that the Early Gate width is also used for Late Gate width. This is done by feedback connections within the address control logic.

Counter Operation. The AUX counter operates similarly to the Transmit and Rec counters. The "all-one's" decode is used to initiate the reload strobes except the reload strobes occupy a complete time slot, consequently, where before, the duration time was N-1 it is now N-2. The all-one's decode is used for generation of the reload strobe when operating from the 10 MHz clock during TX IMP trig generation, when operating from the REC 10 MHz clock for all other pulses. Gates A and B direct this traffic.

Early/Late Gate Shift Register. The shift register on Z3 is used to decode the Early and Late gates. It is clocked from the composite all-one's when allowed by a decode from the address counter. The end of the Late gate is used to turn on a flip-flop. The gate from this flip-flop turns off Gate B and stops the AUX counter operation, otherwise it would continue to make Early and Late gates.

4.5 IF Transversal Equalizer (Hazeltine)

4.5.1 Introduction

This section describes the design approach and theory of operation of the IF Transversal Equalizer.

4.5.2 Description and Theory of Operation

General. The purpose of the transversal equalizer is to suppress time echoes which result from amplitude and phase distortion in the radar transmitter chain, antenna system, or receiver. These distortions are the result of combined component tolerances or may be caused by changes in component electrical characteristics resulting from temperature, pressure, or humidity variations. Additionally, component aging may affect the amplitude and phase transfer function, or the change may be due to the replacement of a major component or assembly. Since the distortion from these effects cannot be precisely predicted, an adjustable transversal equalizer is utilized.

Distortions in the frequency domain result in leading or lagging echoes in the time domain. For a pulse compression radar, these time echoes appear as an increase in the range sidelobe level of the compressed pulse. This results in a degradation in range resolution.

The transversal equalizer employed in this system achieves distortion equalization by an array of fixed taps which provide leading or lagging replicas of the main signal to effect cancellation of distortion echoes. The taps are separated in time by the reciprocal of the instantaneous bandwidth of the received signal. This separation, which is 0.4 usec for the signal bandwidth of 2.5 MHz, satisfies the Nyquist sampling criteria. In addition, the in-phase (I) and quadrature (Q) control of the echo signal, cancellation is effected without the necessity for a moveable tap.

A simplified block diagram of the equalizer is shown in Figure 4-14. The main input signal is divided into two separately delayed paths, one of which contains a fixed delay line (20 μsec) and the other a tapped delay line. Half of the taps have a delay between ten and twenty microseconds while the other half are delays from twenty to thirty microseconds.

Each tap, additionally, has an amplitude (I) and Phase (Q) control which provide for continuous amplitude and 360° phase control of the echo signal.

For a sin X/X input signal, any single tap can generate a replica of the input signal of variable amplitude and carrier phase (0° + 360°). The time occurrence of the echo corresponds to the tap delay. By suitably adjusting any two adjacent taps the echo can be made to slide continuously between the two taps with any desired amplitude and phase.

Theory of Operation

Frequency Domain Analysis. The operation of a transversal equalizer such as that shown in the schematic in Figure 4-15 can be analyzed in either the time or frequency domain. A frequency domain analysis views the radar as a linear transmission system which has a transfer function, H(ω) defined as:

$$H(\omega) = A(\omega)\ 1^{jB(\omega)} \qquad (1)$$

where A(ω) and B(ω) are the steady-state amplitude and phase response, respectively, of the system. For a distortionless system, A(ω) would be a constant (independent of frequency) and B(ω) would be a linear function of frequency.

Deviations from this ideal system can be described by a Fourier series expansion about the frequency band of concern.

$$A(\omega) = a_o + \left[\sum_{n=1}^{N} a_n \cos(nc\omega + \phi)\right] \qquad (2)$$

$$B(\omega) = b_{o\omega} + \left[\sum_{n=1}^{N} b_n \sin(nc\omega) + \phi)\right] \qquad (3)$$

where distortion terms are in brackets. The transversal equalizer when cascaded with the network producing the distortion, must cancel the bracketed terms.

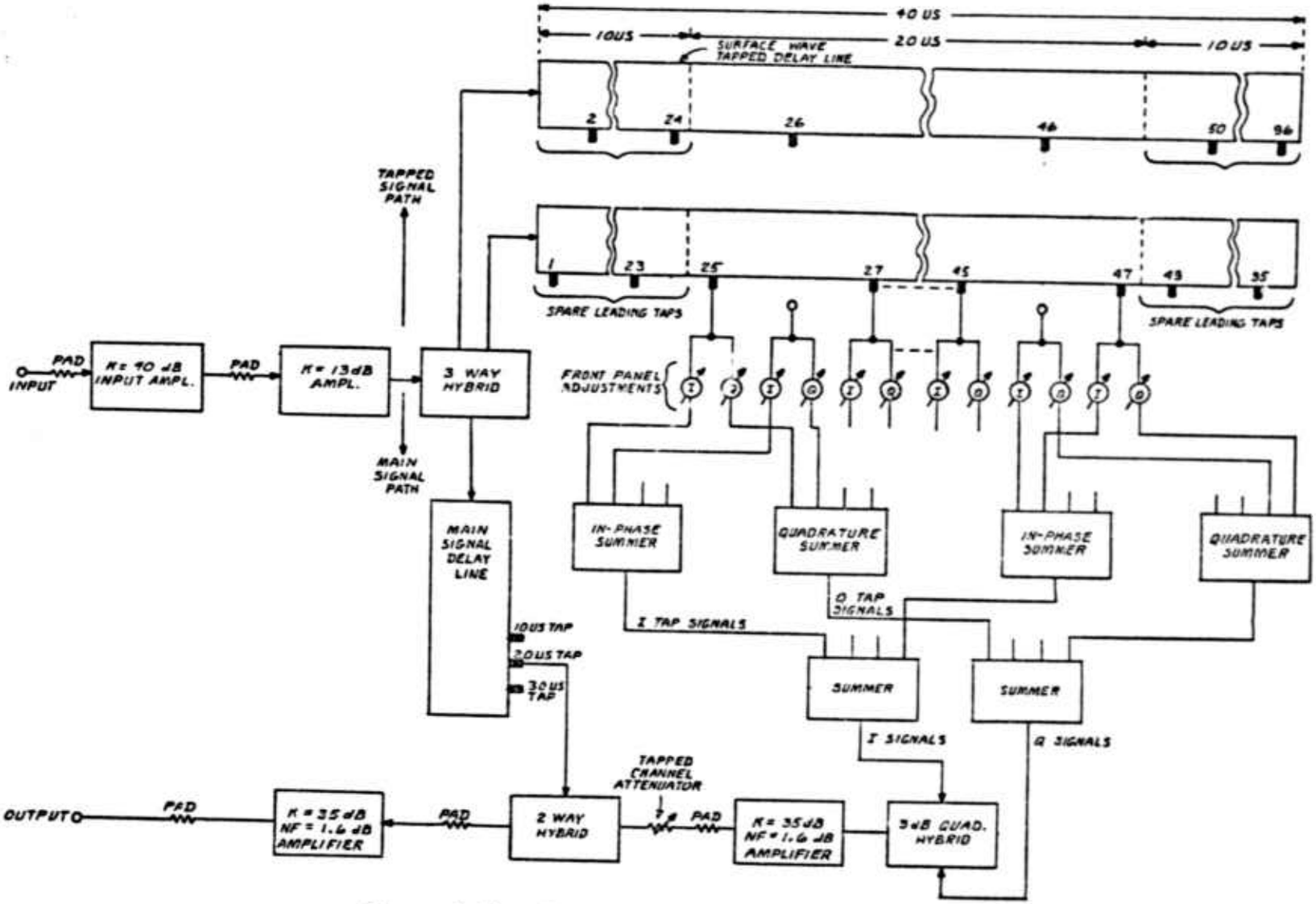


Figure 4.14 Transversal Equalizer Block Diagram

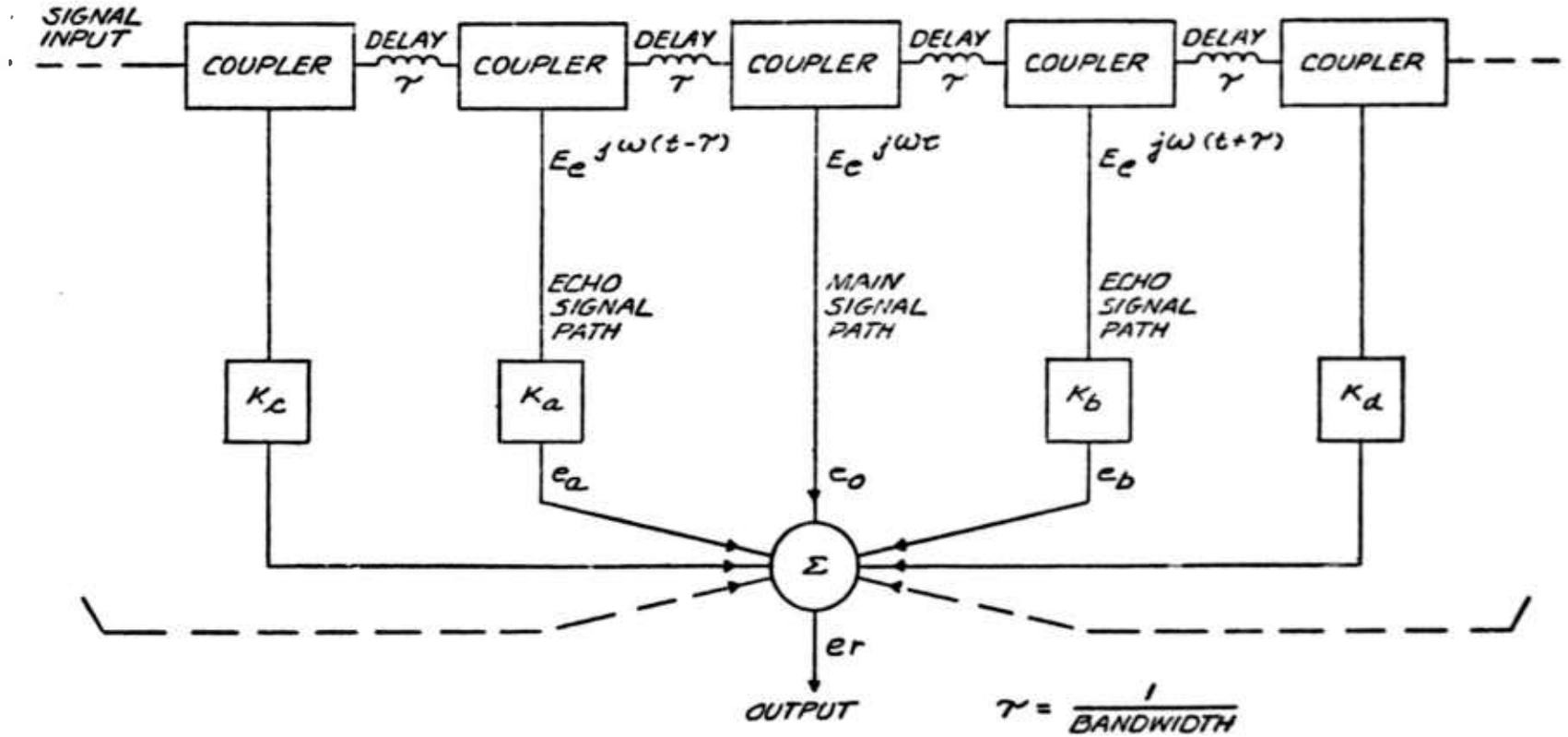


Figure 4.15 Transversal Equalizer System Diagram

Thus, it must be possible to adjust the phase and amplitude to yield terms:

$$A^1(\omega) = K\left[a_o + \sum_{n=1}^{N} a_n \cos(n c\omega + \phi)\right]^{-1} \qquad (4)$$

and

$$B^1(\omega) = b_o^1 \omega - \left[\sum_{n=1}^{N} b_n \sin(n c\omega +)\right] \qquad (5)$$

For the case where the amplitude distortion is small compared to one neper (8.68db), equation (4) can be reduced to the form,

$$A^1(\omega) = k\left[a_o - \sum_{n=1}^{N} a_n \cos(n_{c\omega} + \phi)\right] \qquad (6)$$

The ability of the equalizer to produce independent controllable amplitude and phase terms is shown as follows. The equalizer consists of a tapped delay line as shown in Figure 4-16. The taps are fixed and spaced by γ which is equal to the reciprocal of the bandwidth. The reference is selected as the main output signal I_o.

$$e_o = E_e^{jwt} \qquad (7)$$

The output from tap "a" is:

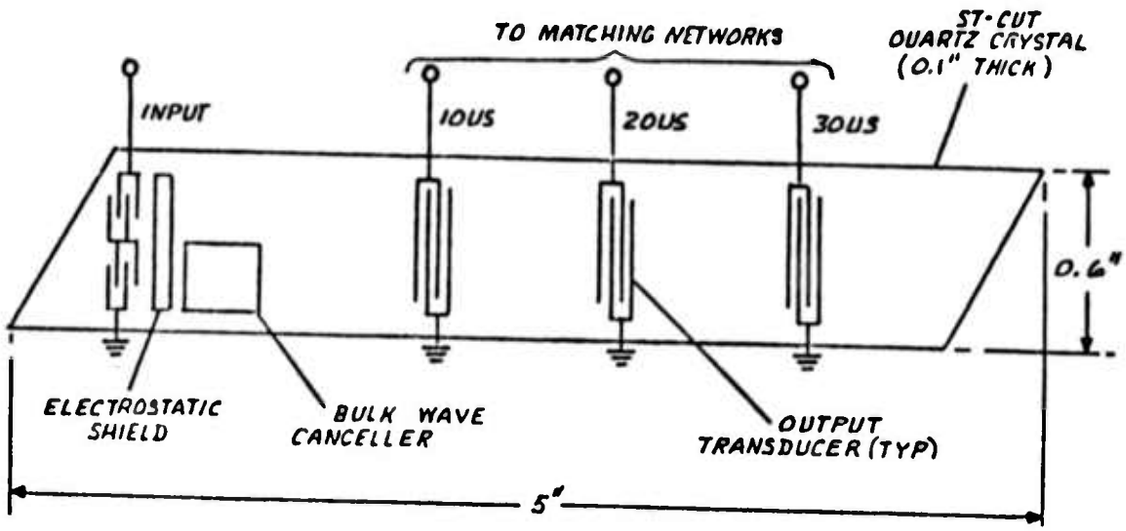
$$e_a = K_a e^{j\omega(t-\gamma)} \qquad (8)$$

and the output from tap "b" is:

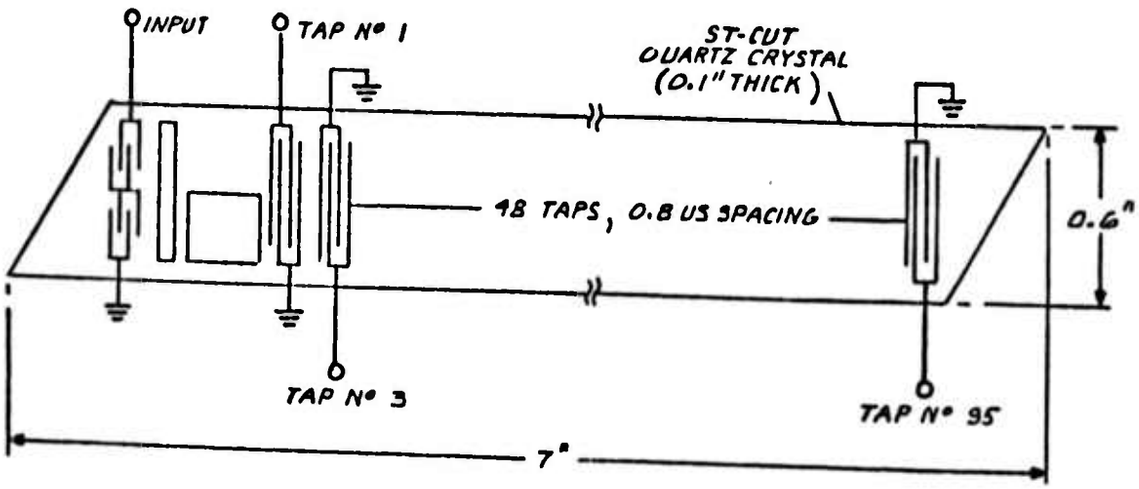
$$e_b = K_b e^{j\omega(t+\gamma)} \qquad (9)$$

Where Ka and Kb are of the form

$$K = \pm e^{-L}$$



(a) MAIN LINE



(b) TAPPED LINE *

NOTE:
TWO TAPPED LINE ARE USED. ONE LINE CONTAINS THE ODD TAPS, THE OTHER LINE THE EVEN TAPS.

Figure 4.16 Delay Lines

Thus, the boxes in Figure 4-15 designated as Ka and Kb can produce attenuation and phase reversal of the leading and lagging signals.

The output signal e_α is

$$e_\alpha = e_o + e_a = e_b$$

$$e_\alpha = E_e^{\,j\omega t} + Ka_e^{\,j\omega(t+\gamma)} + K_b e^{\,j\omega(t+\gamma)}$$

$$e_\alpha = E_e^{\,j\omega t}\left[1 + K_a e^{\,-j\omega t} + K_b e^{\,j\omega\gamma}\right] \qquad (10)$$

By defining, $Ka = Kg + Kp$

and $Kb = Kg - Kp$

then, $e\alpha = E\, e^{\,j\omega t}\left[1 + 2Kg \cos \omega\gamma + J^2 Kp \sin \omega\gamma\right]$ (11)

The condition of Ka=Kb results in the addition of a leading and lagging vector (echo) of equal amplitude and polarity to the main signal. Thus, the sine phase term is zero and only the magnitude of the output signal varies. The output amplitude is a cosine variation with a period of $\omega\gamma$, which fulfills the condition for the Fourier expansion of the error term in equation (6).

When Ka = -Kb, equal but opposite polarity echoes are added to the main vector. This results in a sinusoidal variation of the phase characteristic as a function of frequency which satisfies the condition required by equation (5).

Time Domain Analysis. The time domain and frequency domain are rigourously related by the Fourier transform. However, a much simpler relation is the "paired echo" theory of H.A. Wheeler. This analysis provides substantial insight into the time domain response which results from a prescribed frequency domain error. The analysis is nearly exact for amplitude distortions less than one neper, and phase distortions less than one radian. These conditions generally prevail in a practical wide-band radar system.

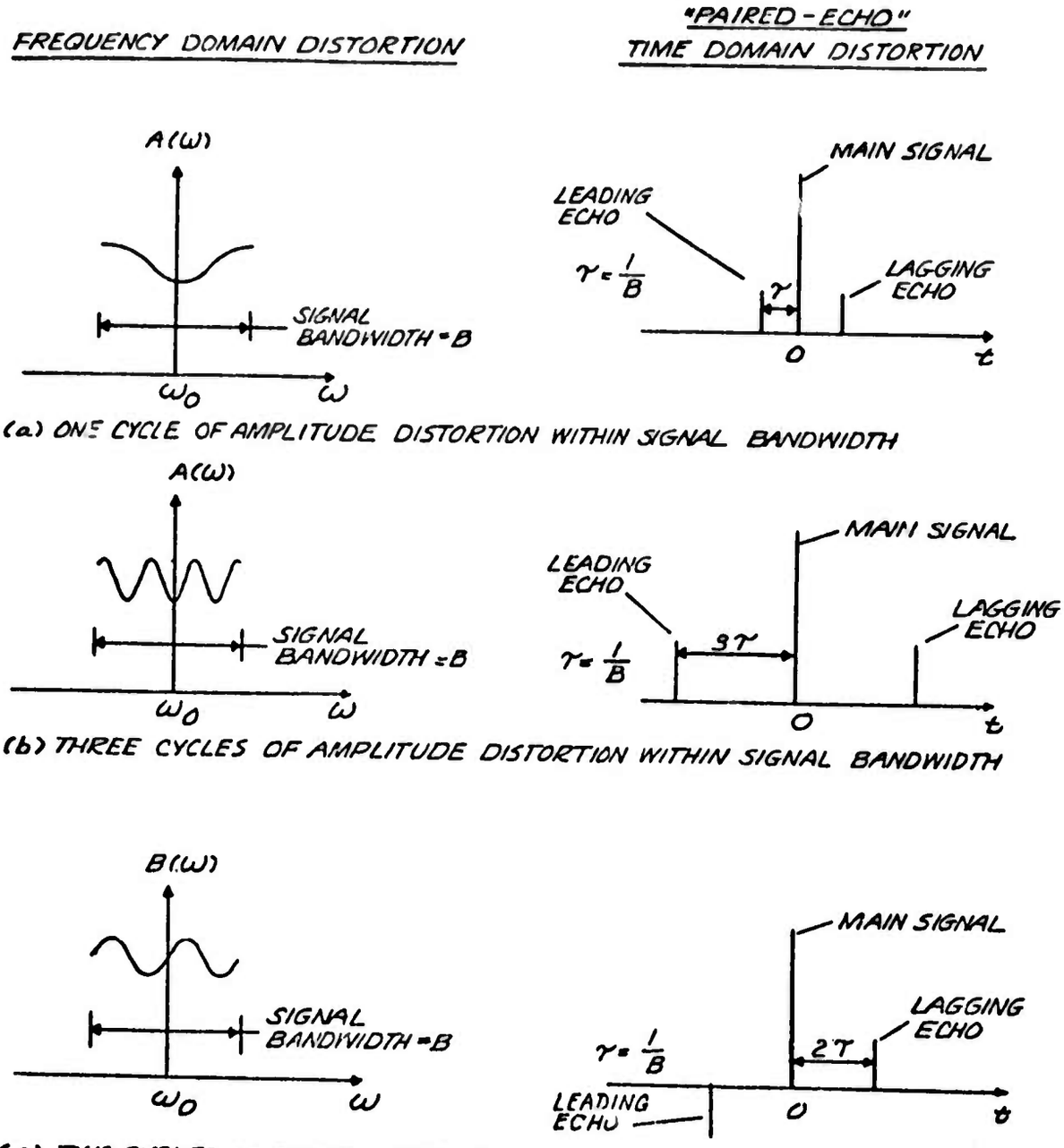


Figure 4.17 Illustration of Paired Echo Theory

Wheeler's paired echo theory predicts that the effect of a sinusoidal amplitude or phase error is to cause symmetrically displaced echoes or replicas of the main signal to appear on either side of the main pulse. The spacing of the echoes from the center of the main pulse is, in time, equal to the reciprocal of the period (frequency) of the error. The magnitude of the echo is proportional to the error amplitude. The theory further predicts that amplitude errors give rise to even symmetry in the output echoes, while phase errors result in echoes having odd symmetry. The "paired-echo" theory is illustrated in Figure 4-17 for several cases of amplitude and phase distortion.

Figure 4-18 shows the relationship between amplitude and phase errors and paired echo sidelobe level. The sidelobe level is shown as a function of the peak deviation of a sinusoidal distortion of amplitude and phase. It is interesting to note that if the amplitude and phase distortions are expressed in nepers and radians, respectively, then equal errors result in equal amplitude echoes. For example, a peak error of 0.1 radians or nepers results in a -25 db sidelobe.

4.5.3 Electrical Parameters

The main electrical parameters of the transversal equalizer are summarized below:

Center Frequency	20 MHz
Signal Bandwidth	2.5 MHz (max.)
Lower 3 db Frequency	17.5 MHz
Upper 3 dB Frequency	22.4 MHz
Distortion Equalization	-40 dB sidelobe level (for weighted signal); sin x/x envelope $\pm$1 dB (for unweighted signal)
Number of Adjustable Taps	48 In-phase 48 Quadrature
Tap Spacing	0.4 μs
Equalized Range Window	18.8 μs
Available Range Window	38.0 μs
Main Signal Delay Relative to Mid-Delay of 18.8 Window	-10 μs, 0, +10 μs (Selectable)
Maximum Input Power (1 dB compression)	-4 dBm
Gain (main channel)	4.5 dB
Noise Output Power (terminated input)	-81.5 dBm
Tapped Channel Amplitude Range	-15 dB to greater than 50 dB below main lobe

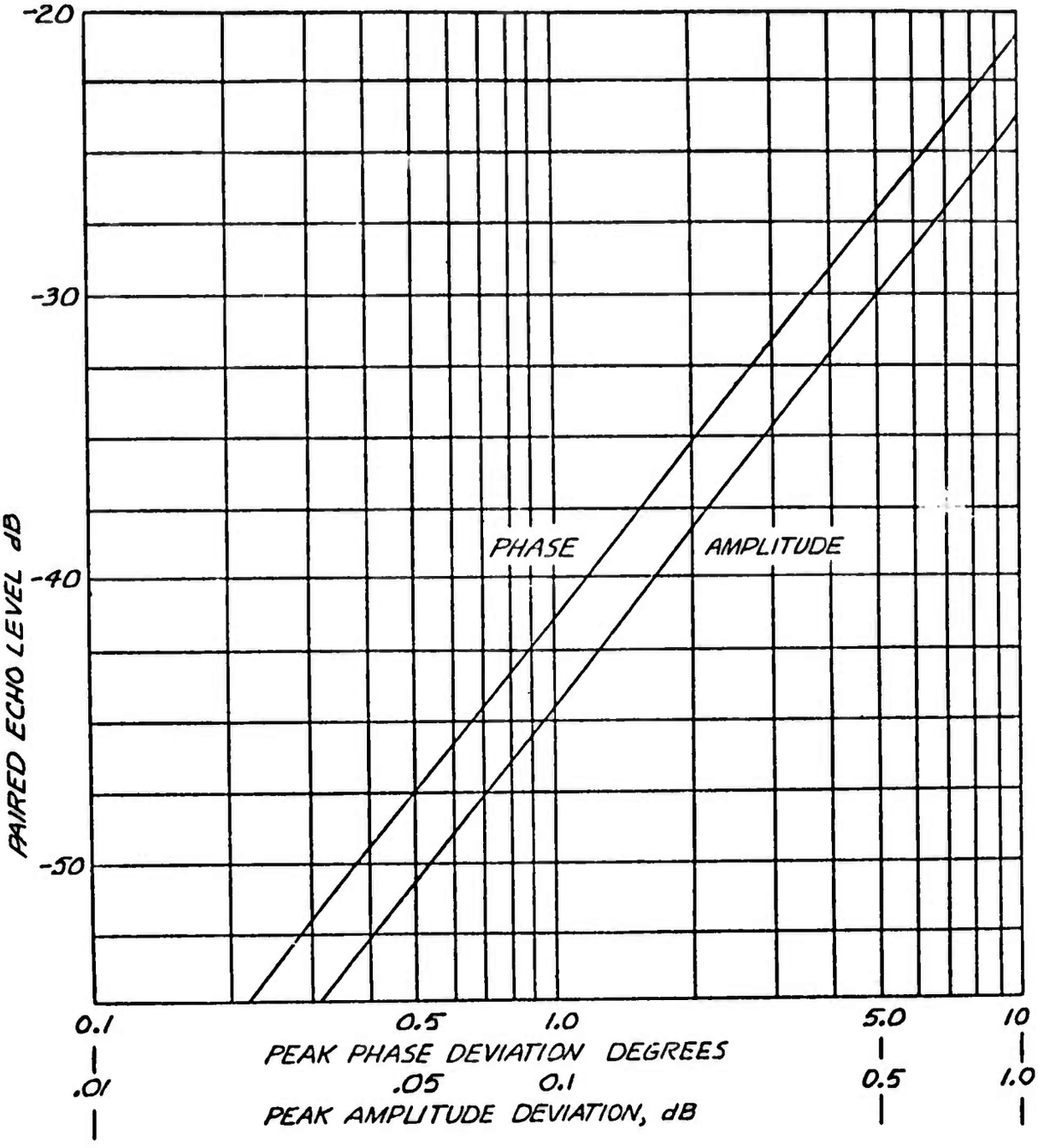


Figure 4.18 Dependence of Paired Echo Level or Magnitude of Amplitude and Phase Distortions

Tapped Channel Phase Range	360°
Spurious Signal Level	-50 dB (max)
Input VSWR (50 ohms)	1.15:1 (max)
Output VSWR (50 ohms)	1.09:1 (max)
D.C. Power	+28 vdc @ 2.6 amps +20 vdc @ 0.1 amps

SECTION 5

SUMMARY AND CONCLUSIONS

The RADC SOI Test Facility has been upgraded to provide the 500 MHz capability that was originally part of the design specifications. Due to the critical performance specifications of components, such as the UP/DOWN converters and the Pulse Compression Network, the vendors failed to meet their delivery schedules and an overall real world system demonstration could not be made prior to contract completion.

However, all the subsystem testing indicated that the facility has the inherent capability to provide low sidelobe levels with a 500 MHz bandwidth and can be used as a wideband CONUS SOI facility as required by the USAF.

REFERENCES

REFERENCE 1 (RCA FOM-12) — REPORT ON EVALUATION TESTS OF SPTF TRANSMITTER PERFORMED AT FLOYD

REFERENCE 2 (RCA FOM-13) — TRIP REPORT - VISIT TO FLOYD SITE W/E 16 MARCH 1973

REFERENCE 3 (RCA FOM-17) — VCO LINEARITY MEASURING TECHNIQUE

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Source AFSCR 23-50, 11 May 70